SOME NEW ADDRESSING TECHNIQUES FOR R M S RESPONDING MATRIX LCDs

A Thesis

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LIST OF ABBREVIATIONS

APT	-	Alt and Pleshko Technique
ASCII	-	American Standard Code for Information Interface
BAT	-	Binary Addressing Technique
BFM	-	Bit-mapped Frame Memory
BPMS	-	Bi-Polar Monopulse Strobe
CD	-	Column Driver
CG	-	Character Generator
CL	-	Control Logic
CMOS	-	Complementary Metal-Oxide Semiconductor
CNPC	-	Cholesteric-Nematic Phase Change
CNPC-GH	-	CNPC-Guest-Host
CSG	-	Column Signal Generator
DAC	-	Digital to Analog Converter
DDF	-	Display Data Formatter
DPC	-	Dye Phase Change
ECB	-	Electrically Controlled Birefringence
EEPROM	-	Electrically Erasable Programmable Read Only Memory
EPROM	-	Erasable Programmable Read Only Memory
FEE	-	Ferro Electric Effect
FIFO	-	First In First Out
FMT	-	Frame Multiplexing Technique (also referred to as SFMT)
GH	-	Guest Host Displays
GHE	-	Guest Host Effect

HAT	-	Hybrid Addressing Technique
HATs	-	Hybrid Addressing Techniques
HST	-	Half-Select Technique
IAPT	-	Improved Alt and Pleshko Technique
IAPT-R	-	IAPT with reduced selection ratio; used for comparing the supply voltage requirement of a technique with IAPT, for the same selection ratio
ICs	-	Integrated Circuits
IHAT	-	Improved Hybrid Addressing Technique
IHAT-S3	-	IHAT - Special case with 3-voltage levels in the column waveforms
IHAT-S4	-	IHAT - Special case with 4-voltage levels in the column waveforms
ITO	-	Indium Tin Oxide
LCDs	-	Liquid Crystal Displays
LM	-	Legend Memory
LSB	-	Least Significant Bit
MIM	-	Metal-Insulator-Metal
MSB	-	Most Significant Bit
NLC	-	Nematic Liquid Crystal
OST	-	One-third Select Technique
PCT	-	Pulse-Coincidence Technique
PRT	-	Pseudo-Random Technique
RAM	-	Random Access Memory
RCR	-	Re-Circulating Register
RD	-	Row Drivers
ROM	-	Read Only Memory
RPAT	-	Restricted Pattern Addressing Technique
RPATs	-	Restricted Pattern Addressing Techniques

RPAT-NC	-	RPAT - Negative Contrast
RPAT-PC	-	RPAT - Positive Contrast
SBAT	-	Switching Bias Voltage Addressing Technique
SBE-Displays	-	Super-twisted Birefringence Displays
SBE-180	-	SBE Display with 180° twist
SBE - 270	-	SBE Display with 270° twist.
SG	-	Sequence Generator
SSE	-	Smectic Storage Effect
STNLCDs	-	Super-Twisted Nematic LCDs (SBE Displays)
TFAT	-	Two Frequency Addressing Technique
TFT	-	Thin Film Transistor
TFMS	-	Two Field Monopulse Strobe
TNFE	-	Twisted Nematic Field Effect
TN-GH	-	Twisted Nematic Guest Host
TNLCDs	-	Twisted Nematic LCDs
UV-EPROM	-	Ultraviolet Erasable Programmable Read Only Memory
VLG	-	Voltage Level Generator
WAM	-	Waveform Acquisition Module
WM	-	Waveform Memory.

LIST OF SYMBOLS

A	-	number of times a pixel gets a favourable voltage during $2^{(N-1)}$ or $2^{(l-1)}$ time intervals
A_i	-	number of times a pixel gets a favourable voltage, when C_i row-select patterns with i mismatches are considered.
A_m	-	see eqn. (3.123) in page 3.55
B	-	number of times a pixel gets an unfavourable voltage during $2^{(N-1)}$ or $2^{(l-1)}$ time intervals considered.
B_i	-	number of times a pixel gets an unfavourable voltage, when C_i row-select patterns with i mismatches are considered.
C_i	-	number of row-select patterns with i mismatches.
C^*_m	-	see eqn. (3.121) in page 3.55.
D	-	see eqn. (3.147) in page 3.63.
E	-	see eqn. (3.148) in page 3.63.
F	-	see eqn. (3.149) in page 3.63.
G	-	see eqn. (3.150) in page 3.63.
K	-	square of the selection ratio (R).
M	-	number of columns in a matrix display, i.e., number of signal electrodes.
N	-	number of address lines multiplexed, i.e., number of scanned lines; number of rows in the matrix display.
N_l	-	Number of leads to the display.
N_{eq}	-	The number of address lines to be multiplexed using APT or IAPT in order to get the same selection ratio as that of the technique being compared.

P	-	Pitch
R	-	Selection ratio
V	-	Reduced voltage normalized to the V_{th}
V_c	-	amplitude of the column (signal) voltage
VDD	-	positive supply voltage
VEE	-	negative supply voltage
V_i	-	amplitude of the column voltage when the number of mismatches is i
V_m	-	amplitude of the column voltage in 1HAT-S3.
V_{m1}	-	amplitude of the column voltage in 1HAT-S4 (see page 3.52).
V_{m2}	-	amplitude of the column voltage in 1HAT-S4 (see page 3.52).
V_r	-	amplitude of the row-select voltage
V_s	-	supply voltage in BAT.
V_{supply}	-	supply voltage requirement of the addressing technique.
V_{sat}	-	saturation voltage (also referred to as V_{90})
V_{th}	-	threshold voltage (also referred to as V_{10})
W	-	Number of selected pixels in a column.

Table 3.7. HAT Vs. IAPT - A comparison

N	l	Selection Ratio (R)		Supply voltage of HAT (normalized to V_{th})	Reduced V_t/V_c of IAPT-R	$\frac{V_{supply}\ HAT}{V_{supply}\ (IAPT\text{-}R)} \times 100\%$
		HAT	IAPT			
3	3	1.732	1.932	2.000	1.000	81.65
6	3	1.447	1.543	2.487	1.415	95.62
5	5	1.483	1.618	1.789	1.214	72.69
10	5	1.312	1.387	2.333	1.718	83.73
15	5	1.246	1.302	2.767	2.105	89.77
20	5	1.209	1.255	3.138	2.432	93.80
25	5	1.184	1.225	3.466	2.714	96.87
30	5	1.167	1.203	3.764	2.981	99.05
7	7	1.382	1.488	1.706	1.400	56.69
14	7	1.252	1.315	2.266	1.977	76.00
21	7	1.200	1.248	2.706	2.422	80.97
28	7	1.171	1.211	3.079	2.794	84.42
35	7	1.151	1.186	3.409	3.132	86.60

3.2.4. Discussion

The merits and demerits of HAT are given in Table 3.8. The HAT extends the BAT for higher values of N and can be considered as an intermediate step between the BAT and the IHAT, discussed in the next section.

3.3. IMPROVED HYBRID ADDRESSING TECHNIQUE (IHAT)

The IHAT proposed in this section is similar to the HAT discussed earlier, except for the choice of the column voltages. This technique has the same selection ratio as that of the conventional APT or IAPT, which is higher than that of HAT. A considerable reduction in the supply voltage requirement is possible in IHAT, as compared to IAPT or APT. In APT, the supply voltage required increases with the number of address lines (N). The IHAT presented here, requires a lower supply voltage as compared to IAPT even when the value of N is large. Important aspects of IHAT are considered in this section.

3.3.1. Background

The number of voltage levels in the column waveform is restricted to just two in BAT and HAT. However, the column voltage can be chosen depending on the number of mismatches (i) between the row-select and the data patterns. The IHAT discussed here, has multiple voltage levels in the column waveform and the choice of the column voltage depends on the value of i. Hence, both the amplitude and the sign of the column voltage depend on the value of i in IHAT, while only the sign of the column voltage is chosen according to the value of i in HAT. This increased freedom results in the following improvements in IHAT as compared to HAT:-

Table 3.3. Merits and Demerits of HAT

Merits	Demerits
- Extension of BAT for high values of N ;	- Selection ratio lower than that of IAPT ;
- Good pixel brightness uniformity ;	- Number of time intervals to complete a cycle higher than IAPT .
- Natural dc-free operation ;	
- Lower supply voltage requirement as compared to IAPT for limited values of N ;	
- High duty cycle as compared to IAPT .	

- A higher selection ratio ;
- A considerable reduction in the supply voltage requirement as compared to lAPT for all values of N by a proper choice in the value of l, and
- The value of l can be odd or even as against odd only in the case of HAT.

3.3.2. Technique

The N rows to be multiplexed in a display are divided into N/l non-intersecting subgroups, each consisting of l address lines. Here again, the data to be displayed in the selected subgroup in any one of the columns is an l-bit word represented by ,

$$d_{kl+1},\ d_{kl+2},\ \cdots,\ d_{kl+l};\quad d_{kl+j} = 0 \text{ or } 1 \qquad (3.49)$$

wherein, logic 0 and logic 1 represent the OFF and ON pixels respectively. The row-select pattern is again an l-bit word represented by,

$$a_{kl+1},\ a_{kl+2},\ \cdots,\ a_{kl+l};\quad a_{kl+j} = 0 \text{ or } 1 \qquad (3.50)$$

The value of k ranges from 0 to $[(N/l) - 1]$ corresponding to the selected subgroups.

The lHAT is similar to HAT except for the choice of the column voltage. The various steps involved in lHAT are given below:-

i) One subgroup is selected at a time for addressing ;
ii) An l-bit word is chosen as the row-select pattern ;
iii) The row-select voltages are $-V_r$ for logic 0 and $+V_r$ for logic 1, while the (N-l) unselected rows are grounded ;

iv) The row-select and the data patterns in the selected subgroup are compared bit-by-bit using digital comparators, viz., exclusive-OR gates ;

v) The number of mismatches i between these two patterns is determined by counting the number of exclusive-OR gates with logic 1 output ;

The steps (iv) and (v) can be summarized as follows:-

$$i = \sum_{j=0}^{l} a_{kl+j} \oplus d_{kl+j} \qquad (3.51)$$

vi) The column voltage is chosen to be V_i, if the number of mismatches is i ;

vii) The column voltage for each column in the matrix is determined independently by repeating the steps (iv) - (vi) ;

viii) Both the row and column voltages are applied simultaneously to the matrix display for a time duration T ;

ix) A new row-select pattern is chosen and the column voltages are determined using steps (iv) - (vi). The new row and column voltages are applied to the display for an equal duration of time at the end of T ;

x) A cycle is completed when all the subgroups ($= N/l$) are selected with all the 2^l row-select patterns once ;

xi) The display is refreshed by repeating this cycle continuously.

The time duration T should be small as compared to the response time of the display, in order to ensure the rms behavior of the display. The

IHAT has the same freedom as in the case of HAT in the choice of the row-select sequence and the subgroup selection as given below:-

- The sequence in which the 2^l row-select patterns are applied to the subgroup can be changed as in the case of BAT.
- A subgroup can be selected with 2^j row-select patterns consecutively before selecting the next subgroup. Here, j can range from 0 to l.
- The order in which the subgroups are selected can also be changed as long as all the subgroups are selected with all the 2^l row-select patterns.

The rms voltages across similar pixels are equal in all the cases discussed above, but the frequency components are different in each case. One of these combinations can be chosen as the addressing sequence to suit the display characteristics.

The column voltage V_i for the various values l and i are given in Table 3.9. The column voltages here are normalized to V_o. Adressing waveforms of IHAT with $l = 2$ and 3 are shown in Fig.3.4 and 3.5 respectively, as typical examples. The natural dc-free operation of IHAT is evident from the waveforms across the pixels illustrated in Fig. 3.4.

3.3.3. Analysis

Let $-V_r$ and $+V_r$ be the row-select voltages of the l-bit word. The (N-l) rows in the unselected subgroups are grounded. Let the column voltage be V_i, corresponding to the i mismatches between the row-select and column voltages. Let the sign of the column voltage be in-phase with the row-select

Table 3.9. Column voltages of lHAT for various values of l and i

l	Column voltages corresponding to number of mismatches i=							
	0	1	2	3	4	5	6	7
2	-1	0	+1	-	-	-	-	-
3	-1	$-\frac{1}{3}$	$+\frac{1}{3}$	+1	-	-	-	-
4	-1	$-\frac{1}{2}$	0	$+\frac{1}{2}$	+1	-	-	-
5	-1	$-\frac{3}{5}$	$-\frac{1}{5}$	$+\frac{1}{5}$	$+\frac{3}{5}$	+1	-	-
6	-1	$-\frac{4}{6}$	$-\frac{2}{6}$	0	$+\frac{2}{6}$	$+\frac{4}{6}$	+1	-
7	-1	$-\frac{5}{7}$	$-\frac{3}{7}$	$-\frac{1}{7}$	$+\frac{1}{7}$	$+\frac{3}{7}$	$+\frac{5}{7}$	+1

Table 3.10. Supply voltage requirements of lHAT Vs. APT for $N > l^2$

No. of address lines in a subgroup	$\frac{V_{supply}(lHAT)}{V_{supply}(APT)} \times 100\%$
2	70.71
3	57.74
4	50.00
5	44.72
6	40.82
7	37.50

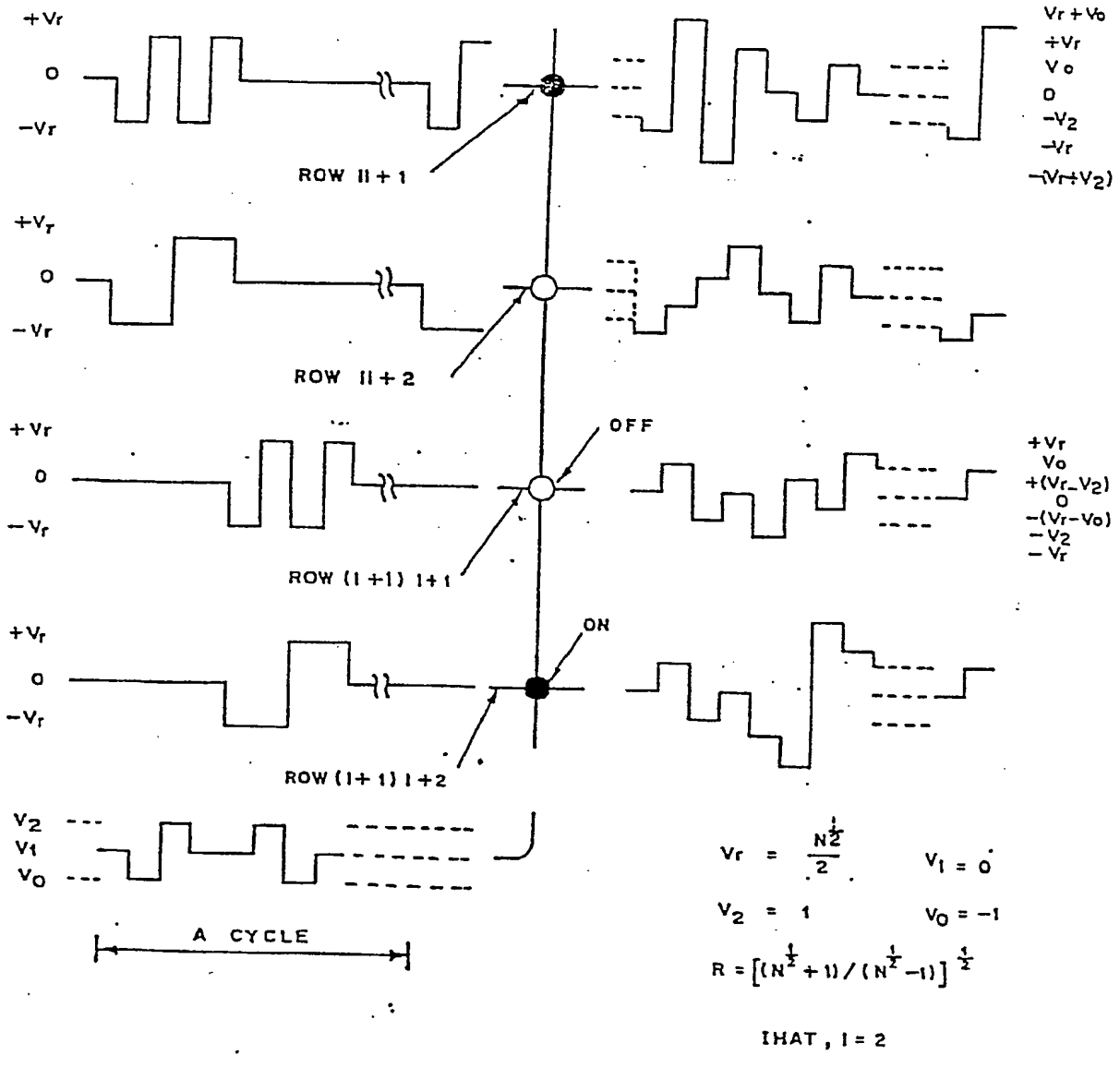


Fig. 3.4. Typical addressing waveforms of IHAT, when $l = 2$.

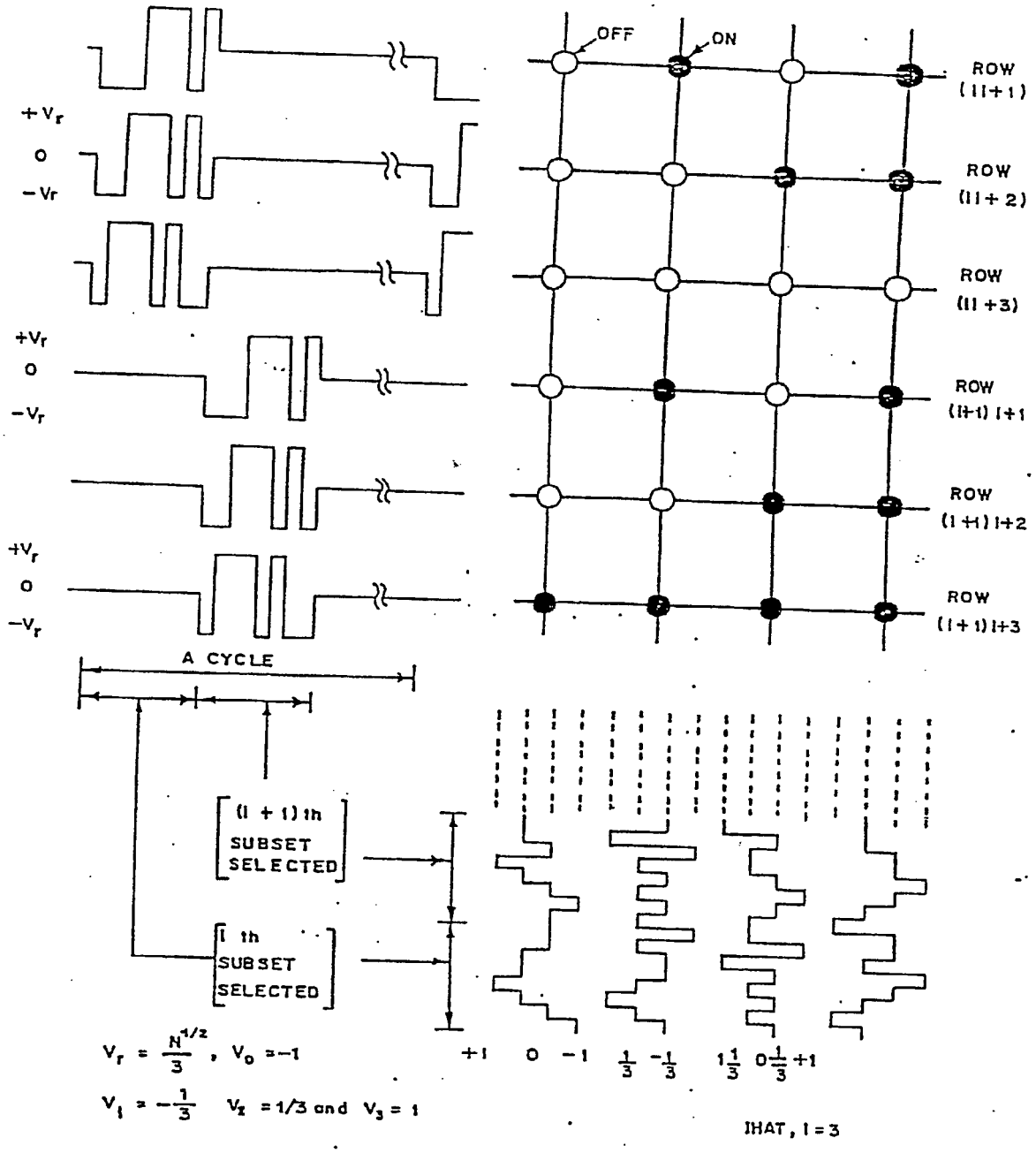


Fig. 3.5. Typical addressing waveforms of IHAT, when I = 3.

voltage corresponding to logic 0. The instantaneous voltage across the pixels are either $|V_r + V_i|$ or $|V_r - V_i|$.

The number of times the l-bit row-select and data patterns differ by i bits is based on eqn.(3.5). Thus,

$$C_i = \frac{l!}{i!(l-i)!} \qquad (3.52)$$

The number of times a pixel gets a favourable voltage, when the number of mismatches in the column is i is based on eqn. (3.9) as given below:-

$$A_i = \frac{(l-1)!}{i!(l-i-1)!} \qquad (3.53)$$

Similarly, the number of times a pixel gets an unfavourable voltage or error, within the C_i row-select patterns considered is given below:-

$$B_i = \frac{i(l-1)!}{i!(l-i)!} \qquad (3.54)$$

The ON pixels get a voltage of $|V_r + V_i|$ during A_i time intervals and a voltage $|V_r - V_i|$ during B_i time intervals out of the total C_i $(= A_i + B_i)$ time intervals considered, when the corresponding row is selected. These pixels also get a voltage $|V_i|$ during $(\frac{N}{l} - 1)C_i$ time intervals, when the corresponding row is unselected. The rms voltage across the ON pixel is determined by summing these voltages for all possible value of mismatches, i.e., summation over i from 0 to l, as follows:-

$$V_{ON}^2(rms) = \left[\sum_{i=0}^{l} A_i(V_r+V_i)^2 + \sum_{i=0}^{l} B_i(V_r-V_i)^2 + \sum_{i=0}^{l} (\frac{N}{l} - 1)(A_i+B_i)\, V_i^2\right] \Big/ (2^l N/l) \qquad (3.55)$$

The rms voltage across an OFF pixel can be arrived at in a similar way as follows:-

$$V_{OFF}^2(rms) = \left| \sum_{i=0}^{l} A_i(V_r - V_i)^2 + \sum_{i=0}^{l} B_i(V_r + V_i)^2 + \sum_{i=0}^{l} \left(\frac{N}{l} - 1\right)(A_i + B_i)V_i^2 \right| \Big/ (2^l N/l) \quad (3.56)$$

The ratio V_{ON}/V_{OFF} should be a maximum in order to achieve a good contrast in the display.

$$\left[\frac{V_{ON}(rms)}{V_{OFF}(rms)}\right]^2 = \frac{\sum_{i=0}^{l}(A_i+B_i)V_r^2 + \frac{N}{l}\sum_{i=0}^{l}(A_i+B_i)V_i^2 + 2\sum_{i=0}^{l}(A_i-B_i)V_rV_i}{\sum_{i=0}^{l}(A_i+B_i)V_r^2 + \frac{N}{l}\sum_{i=0}^{l}(A_i+B_i)V_i^2 - 2\sum_{i=0}^{l}(A_i-B_i)V_rV_i} \quad (3.57)$$

This ratio is of the form

$$\left[\frac{V_{ON}}{V_{OFF}}\right]^2 = \frac{\delta_1 + \delta_2}{\delta_1 - \delta_2} \quad (3.58)$$

where,

$$\delta_1 = V_r^2 \sum_{i=0}^{l}(A_i + B_i) + \left(\frac{N}{l}\right)\sum_{i=0}^{l}(A_i + B_i)V_i^2 \quad (3.59)$$

and

$$\delta_2 = 2V_r \sum_{i=0}^{l}(A_i - B_i)V_i \quad (3.60)$$

The following equations must be satisfied for obtaining an optimum selection ratio.

$$\delta_1 - \delta'_{2V_r} = \delta'_{1V_r} \cdot \delta_2 \quad (3.61)$$

and

$$\delta_1 - \delta'_{2V_i} = \delta'_{1V_i} \cdot \delta_2 \quad \text{for} \quad i = 0 \text{ to } l \quad (3.62)$$

where,

$$\delta'_{1V_r} = 2V_r \sum_{i=0}^{l}(A_i + B_i) \quad (3.63)$$

$$\delta'_{1V_i} = 2\left(\frac{N}{l}\right).(A_i + B_i) \cdot V_i \quad (3.64)$$

$$\delta'_{2V_r} = 2 \sum_{i=0}^{l} (A_i - B_i) V_i \qquad (3.65)$$

and

$$\delta'_{2V_i} = 2V_r(A_i - B_i) \qquad (3.66)$$

The following relation is obtained by substituting for δ_2, δ'_{1V_r} and δ'_{2V_r} in eqn.(3.61)

$$\delta_1 \cdot 2 \sum_{i=0}^{l} (A_i - B_i)V_i = \left[2V_r \sum_{i=0}^{l} (A_i + B_i)\right] 2V_r \sum_{i=0}^{l} (A_i - B_i)V_i \qquad (3.67)$$

or

$$\delta_1 = 2V_r^2 \sum_{i=0}^{l} (A_i + B_i) \qquad (3.68)$$

The following relation is well known from the properties of binomial coefficients:-

$$\sum_{i=0}^{l} (A_i + B_i) = \sum_{i=0}^{l} C_i = \sum_{i=0}^{l} \frac{l!}{i!(l-i)!} = 2^l \qquad (3.69)$$

Hence,

$$\delta_1 = 2^{(l+1)} V_r^2 \qquad (3.70)$$

The following equations are obtained by substituting for δ'_{1V_i} and δ'_{2V_i} in eqns. (3.62)

$$\delta_1 2V_r(A_i - B_i) = 2\frac{N}{l}(A_i + B_i)V_i\delta_2 \qquad \text{for all } i\text{'s} \qquad (3.71)$$

Hence,

$$\frac{(A_i - B_i)}{(A_i + B_i)V_i} = \frac{2N\delta_2}{2lV_r\delta_1} = \text{constant for all } i\text{'s} \qquad (3.72)$$

A relation between the column voltages for i and j mismatches can be obtained, since the term on the right hand side is a constant in the above equation. Hence,

$$\frac{(A_i - B_i)}{(A_i + B_i)V_i} = \frac{(A_j - B_j)}{(A_j + B_j)V_j} \qquad (3.73)$$

or

$$\frac{V_i}{V_j} = \frac{(A_i - B_i)(A_j + B_j)}{(A_i + B_i)(A_j - B_j)} \qquad (3.74)$$

The column voltages can be normalized with any one of the column voltages. However, it is convenient to normalize them to V_o, i.e., the column voltage corresponding to zero mismatches. Substituting for A_0 (=1) and B_0 (=0) in eqn. (3.74), the column voltage for i mismatches is,

$$V_i = \frac{(A_i - B_i)}{(A_i + B_i)} V_o \qquad (3.75)$$

This can be further simplified by substituting for A_i and B_i from eqns. (3.53) and (3.54). Hence,

$$V_i = \frac{(l - 2i)}{l} V_o \qquad (3.76)$$

It can be shown (Appendix 3.a) that

$$V_{(l-i)} = - V_i \qquad (3.77)$$

Hence, the column voltages for i and (l-i) mismatches have the same amplitude and they differ only in phase (sign). The number of errors in a column is made to be the same for i and (l-i) mismatches in both BAT and HAT by a proper choice of the polarity of the column voltage. A similar condition is imposed here by eqn. (3.77).

The equation (3.68) can be rewritten as follows by substituting for δ_1 from eqn. (3.59):-

$$U_r^2 \sum_{i=0}^{l} (A_i + B_i) = \frac{N}{l} \sum_{i=0}^{l} (A_i + B_i) U_i^2 \qquad (3.78)$$

However, U_i^2 is obtained from eqn. (3.75) as follows:-

$$U_i^2 = \frac{(A_i - B_i)^2}{(A_i + B_i)^2} U_o^2 \qquad (3.79)$$

Hence, the eqn. (3.78) becomes

$$U_r^2 \sum_{i=0}^{l} (A_i + B_i) = \frac{N}{l} \sum_{i=0}^{l} \frac{(A_i - B_i)^2}{(A_i + B_i)} U_o^2 \qquad (3.80)$$

The following relation is obtained by substituting for A_i and B_i from eqns. (3.53) and (3.54) in the above equation.

$$U_r^2 \sum_{i=0}^{l} \frac{l!}{i!(l-i)!} = \frac{N}{l^2} U_o^2 \sum_{i=0}^{l} \frac{(l-1)!\,(l-2i)^2}{i!\,(l-i)!} \qquad (3.81)$$

It can be shown (Appendix 3b) that

$$\sum_{i=0}^{l} \frac{l!}{i!(l-i)!} = \sum_{i=0}^{l} \frac{(l-1)!\,(l-2i)^2}{i!\,(l-i)!} = 2^l \qquad (3.82)$$

Hence,

$$U_r^2 = \frac{N}{l^2} U_o^2 \qquad (3.83)$$

The selection ratio is a maximum for the following conditions:-

$$U_r = + \frac{N^{1/2}}{l} U_o \qquad (3.84)$$

and

$$U_i = \left(\frac{l-2i}{l}\right) U_o \qquad (3.85)$$

The function f_2 from eqn.(3.60) can be modified to the following form by

substituting for V_i in terms of A_i and B_i using eqn. (3.75). Thus,

$$\delta_2 = 2V_r \sum_{i=0}^{l} (A_i - B_i)V_i = 2V_r V_o \sum_{i=0}^{l} \frac{(A_i - B_i)^2}{(A_i + B_i)} \qquad (3.86)$$

It can be shown (Appendix 3.c) that

$$\sum_{i=0}^{l} \frac{(A_i - B_i)^2}{(A_i + B_i)} = \frac{2^l}{l} \qquad (3.87)$$

Hence,

$$\delta_2 = 2V_r V_o \left(\frac{2^l}{l}\right) \qquad (3.88)$$

Substituting for V_r using eqn. (3.84),

$$\delta_2 = 2^{l+1} \frac{N^{1/2}}{l^2} V_o^2 \qquad (3.89)$$

The selection ratio is obtained by substituting for δ_1 and δ_2 using eqns. (3.70) and (3.89) in eqn. (3.58)

$$\left[\frac{V_{ON}\ (rms)}{V_{OFF}\ (rms)}\right]^2 = \left[\frac{2^{l+1}\frac{N}{l^2}V_o^2 + 2^{l+1}\frac{N^{1/2}}{l^2}V_o^2}{2^{l+1}\frac{N}{l^2}V_o^2 - 2^{l+1}\frac{N^{1/2}}{l}V_o^2}\right] \qquad (3.90)$$

or

$$R = \frac{V_{ON}\ (rms)}{V_{OFF}\ (rms)} = \left[\frac{N^{1/2} + 1}{N^{1/2} - 1}\right]^{1/2} \qquad (3.91)$$

The selection ratio here, is the same as that of the APT or IAPT. This is the maximum value possible for any addressing technique [69]. However, the complexity of the column waveform is more in IHAT, since the number of column voltages is (l+1) instead of just 2 in HAT. The sign of the column voltage V_i is assumed to be in-phase with the row-select voltage correspon-

ding to logic 0. The column voltages are normalized to V_o, where $-V_r$ is for logic 0 and $+V_r$ is for logic 1 in the l-bit row-select pattern. This is given in Table 3.9.

The rms voltages across the ON and OFF pixels, when the selection ratio is a maximum are as follows:-

$$V_{ON}\,(rms) = \left[\frac{2^{l+1}\,V_o^2(N + N^{1/2})\,l}{l^2\,2^l\,N}\right]^{1/2} = \left[\frac{2(N + N^{1/2})}{Nl}\right]^{1/2} V_o \qquad (3.92)$$

and

$$V_{OFF}\,(rms) = \left[\frac{2^{l+1}V_o^2(N - N^{1/2})\,l}{l^2\;2^l\;N.}\right]^{1/2} = \left[\frac{2(N - N^{1/2})}{Nl}\right]^{1/2} V_o \qquad (3.93)$$

The OFF pixels in the display are biased near V_{th} in order to obtain a good contrast ratio. Hence,

$$V_{OFF} = V_{th} \qquad (3.94)$$

or

$$V_o = \left[\frac{N.l}{2(N - N^{1/2})}\right]^{1/2} V_{th} \qquad (3.95)$$

ne supply voltage requirement is determined by the maximum swing in the addressing waveforms. The amplitude of the row select voltage (V_r) is lower than V_o for $N < l^2$, is the same as V_o for $N = l^2$ and is greater than V_o for $N > l^2$. The column voltages for $i \geq 0$ are however lower or equal to V_o (Table 3.9). Hence, the supply voltage of 1HAT is calculated for two ranges of N as given below:-

$$V_{supply}\,(1HAT) = 2V_o \qquad \text{for } N \leq l^2 \qquad (3.96)$$

and

$$V_{supply\ (1HAT)} = 2V_r = 2\frac{N^{1/2}}{l} V_o \quad \text{for } N \geq l^2 \tag{3.97}$$

Hence,

$$V_{supply\ (1HAT)} = \left[\frac{4l}{2(1 - N^{-1/2})}\right]^{1/2} V_{th} \quad \text{for } N \leq l^2 \tag{3.98}$$

and

$$V_{supply\ (1HAT)} = \left[\frac{4(N/l)}{2(1 - N^{-1/2})}\right]^{1/2} V_{th} \quad \text{for } N \geq l^2 \tag{3.99}$$

The supply voltage of APT for a comparison is obtained from eqn. (2.17) as follows:-

$$V_{supply\ (APT)} = \left[\frac{2N^{1/2}}{[2(1 - N^{-1/2})]^{1/2}}\right] = \left[\frac{4N}{2(1 - N^{-1/2})}\right]^{1/2} \tag{3.100}$$

The supply voltage requirement of 1HAT is compared with that of APT using the following ratio:-

$$\frac{V_{supply\ (1HAT)}}{V_{supply\ (APT)}} = \begin{cases} \left(\frac{l}{N}\right)^{1/2} & \text{for } N \leq l^2 \\ \left(\frac{1}{l}\right)^{1/2} & \text{for } N \geq l^2 \end{cases} \tag{3.101}$$

It is evident that this ratio is independent of N, when $N \geq l^2$. This condition can be met with a proper choice of l for a given N. The supply voltage requirements of 1HAT for various values of l ($N \geq l^2$) are compared with that of APT in Table 3.10. From this table, it is clear that 1HAT requires a lower supply voltage as compared to APT.

The 1APT is popular at present, due to its lower supply voltage requirement as compared to the APT. Hence, the supply voltage of 1HAT is also compared with that of 1APT.

The supply voltage of 1APT is recalled from equation (2.18)

$$V_{supply}\ (1APT) = \frac{(N^{1/2} + 1)}{[2(1 - N^{-1/2})]^{1/2}} \qquad (3.102)$$

Hence,

$$\frac{V_{supply}\ (1HAT)}{V_{supply}\ (1APT)} = \begin{cases} \dfrac{2\ell^{1/2}}{(N^{1/2} + 1)} & \text{for } N \leq \ell^2 \\ \dfrac{2(N/\ell)^{1/2}}{(N^{1/2} + 1)} & \text{for } N \geq \ell^2 \end{cases} \qquad (3.103)$$

The supply voltage requirement of 1HAT is compared with that of 1APT for various values of N and ℓ in Figs. 3.6 and 3.7. The following points are evident from these figures :-

- The reduction in the supply voltage is maximum when $N = \ell^2$, and
- It is possible to achieve a considerable reduction in the power supply voltage as compared to 1APT by a proper choice of the value of ℓ.

Table 3.11 gives the value of ℓ leading to a good reduction in the supply voltage for a wide range of values of N. From this table it is clear that 'HAT with $\ell = 7$ is quite adequate for a wide range, especially for high values of N ($N > 49$). The supply voltage increases with N in general. It is important to note that 1HAT requires a considerably lower supply voltage as compared to 1APT, even when a few thousand lines are multiplexed.

3.3.4. Discussion

The merits and demerits of 1HAT as compared to 1APT are given in Table 3.12. 1HAT requires a lower supply voltage as compared to 1APT,

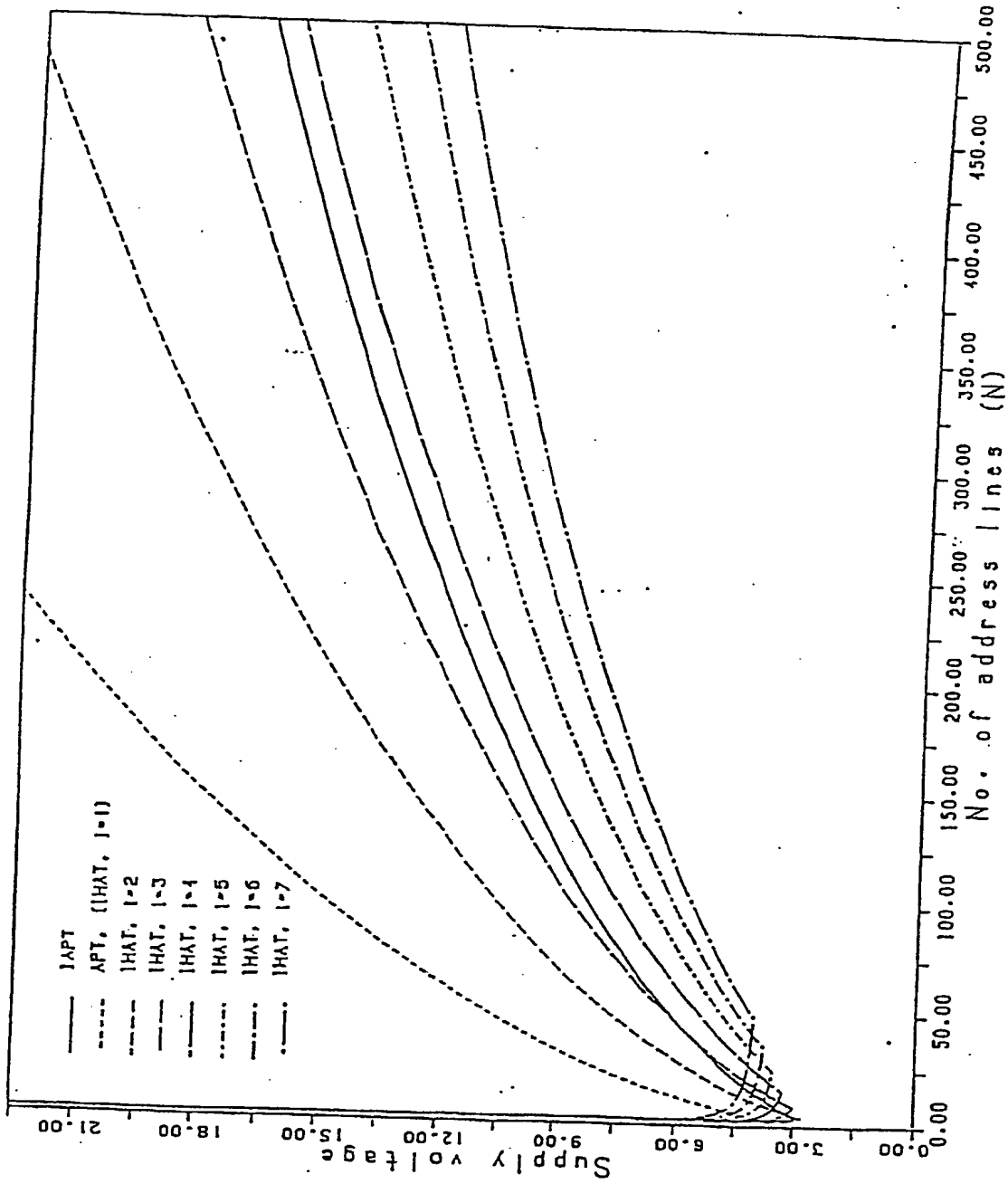


Fig. 3.6. Supply voltage (normalized to V_{th}) vs. N for both IHAT and IAPT.

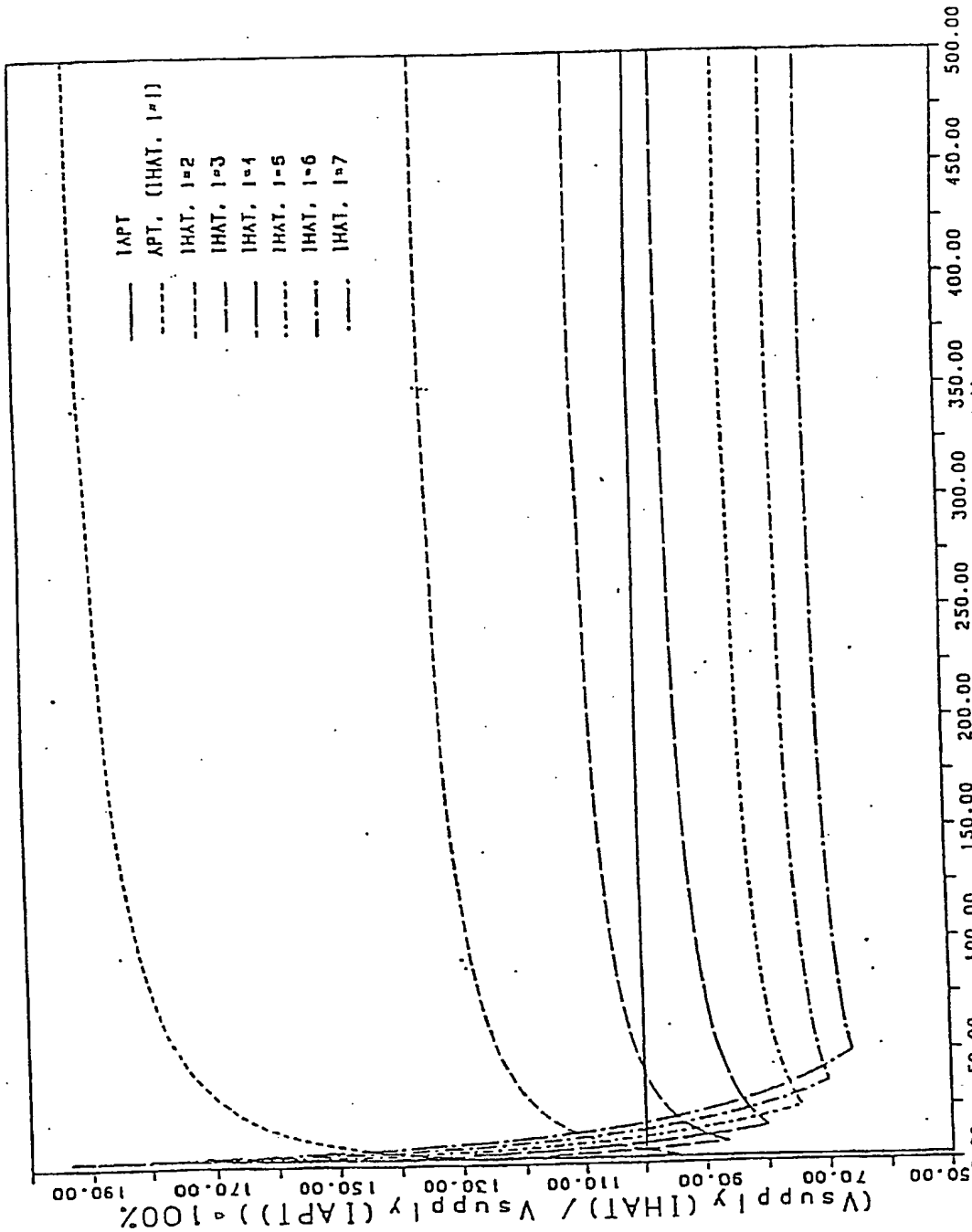


Fig. 3.7. A comparison of supply voltage requirement of IHAT with that of IAPT.

Table 3.11. Possible values of l, for different N leading to a good reduction in the supply voltage requirement

N	l	$\frac{V_{supply}\ (IHAT)}{V_{supply}\ (IAPT)} \times 100\%$ V_{th} constant	No. of voltage levels in the addressing waveforms	No. of time intervals in a cycle of (IHAT)/(IAPT)
4	2	94.28	3	1
9	3	86.60	5	4/3
12	3,4	89.60	7,8	4/3, 8/4
16	4	80.00	5	8/4
20	4,5	81.73	8,9	8/4, 16/5
25	5	74.54	7	16/5
30	5,6	75.63	9,10	16/5, 32/6
36	6	69.99	7	32/6
42	6,7	70.74	10,11	32/6, 64/7
49	7	66.14	9	64/7
70	7	67.52	11	64/7
140	7	69.70	11	64/7
280	7	71.33	11	64/7
560	7	72.59	11	64/7
1120	7	73.40	11	64/7
2240	7	74.03	11	64/7
4480	7	74.48	11	64/7

Table 3.12. Merits and Demerits of IHAT as compared to IAPT

Merits
- Good reduction in supply voltage possible by proper choice in the value of l ;
- Better pixel brightness uniformity by choosing scanning sequence to match display characteristics ;
- Natural dc-free operation ;
- Higher duty cycle .
Demerits
- Number of voltage levels in the column waveforms is $(l+1)$ against four in IAPT ;
- Number of time intervals to complete a cycle higher by a factor $[2^{(l-1)}/l]$.

especially for a high value of N. However, the hardware complexity of 1HAT increases with l, since (l+1) switches are required in each column driver to generate the column waveforms.

3.4. 1HAT - SPECIAL CASES (1HAT-S)

The 1HAT presented in the previous section is well suited for multiplexing TNLCDs, wherein the selection ratio is an important parameter. However, displays based on SBE exhibit steep electro-optic characteristics. Hence, a selection ratio lower than that of 1HAT or 1APT is acceptable here. This facilitates a reduction in the hardware as the number of voltage levels in the column waveform can be restricted as in the case of HAT. The trade-off between the hardware complexity and the resulting selection ratio as well as the supply voltage requirement is analyzed in this section.

3.4.1. Background

The number of voltage levels in the column waveform (n_c) can be restricted by grouping the number of mismatches (i) and assigning a column voltage for each group. The value of n_c can be restricted to 3 in the case of even l and 4 in the case of odd l instead of (l+1) in the case of 1HAT. This leads to a lower selection ratio as compared to that of 1HAT. An optimum grouping of mismatches with a minimum degradation in the selection ratio, can be arrived at by an exhaustive search of all the possible groupings for each l.

3.4.2. Techniques

The technique for even values of l will be referred to as 1HAT-S3, since the number of column voltages is restricted to 3 here. This technique

is similar to 1HAT except for the choice of a column voltage (V_c) as given below:-

$$V_c = \begin{cases} -V_m & \text{for } 0 \leq i \leq m \\ 0 & \text{for } m < i < (l-m) \\ +V_m & \text{for } (l-m) \leq i \leq l \end{cases} \quad (3.104)$$

The number of column voltages is restricted to 4 in the case of odd values of l and will be referred to as 1HAT-S4. Here again, the technique is similar to 1HAT except for the choice of a column voltage (V_c) as given below:-

$$V_c = \begin{cases} -V_{m1} & \text{for } 0 \leq i \leq m1 \\ -V_{m2} & \text{for } m1 < i < (l/2) \\ +V_{m2} & \text{for } (l/2) < i < (l-m1) \\ +V_{m1} & \text{for } (l-m1) \leq i \leq l \end{cases} \quad (3.105)$$

3.4.3. Analysis

Case 1: 1HAT-S3

Three groups, covering the range 0 to l are formed when the value of l is even and are represented as given below:-

$$(0,1,\ldots,m)\ ;\ (m+1,\ldots\ldots,l-m-1)\ ;\ (l-m\ ;\ \ldots\ldots,\ l) \quad (3.106)$$

The number of entries in the first and the last group are chosen to be equal here since the number of errors can be minimized by a proper choice of the polarity of the column voltage. This is similar to the other techniques discussed earlier.

Let the column voltages be V_{g1}, V_{g2} and V_{g3} respectively for the three groups. The following constraints are imposed on these voltages based

CHAPTER 4

EXPERIMENTAL WORK

4. EXPERIMENTAL WORK

A number of new addressing techniques for multiplexing matrix LCDs with rms response have been proposed in the previous chapter, along with the theoretical analysis in each case. The hardware realization of some of these techniques, viz., BAT, HAT, IHAT, IHAT-S4, RPAT-NC and RPAT-PC is taken up in this chapter, in view of the importance of the same. The block diagrams of the display systems using these addressing techniques and the approach to their realization are discussed first. This is followed by the details of the implementation and discussion of the results obtained by using these techniques.

4.1 APPROACH TO REALIZATION

4.1.1. BAT

The BAT is suitable for single row alphanumeric displays, where the number of lines to be multiplexed (N) is small (Appendix 6.a).

a) Block diagram

The block diagram of a display system using BAT is shown in Fig.4.1. The character information is stored in the memory. The standard ASCII code is used for storing the alphanumeric characters to be displayed. This information in the memory is updated through the interface, which connects the display to an input equipment (computer, keyboard, etc.) depending on the application. The Character Generator (CG) converts the ASCII code to pixel information. A column-wise output is required for the BAT. The 2^N row-select patterns required for BAT are obtained from the Sequence

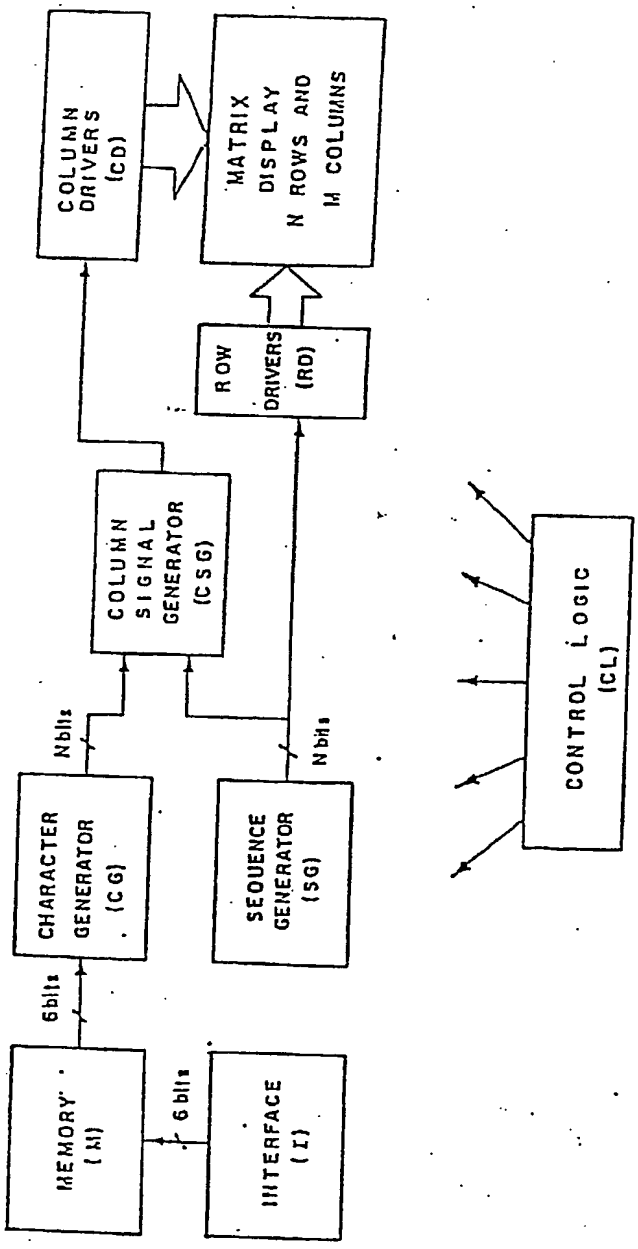


Fig.4.1. Block diagram of display system using BAT.

Generator (SG). The Column Signal Generator (CSG) compares the data from the CG and the row-select pattern from SG bit-by-bit and generates the data for the Column Drivers (CD). This requires a majority decision as discussed in section 3.1.2. The Row Drivers (RD) obtain the row-select pattern from SG. The row-select pattern and the column data should be simultaneously applied to the matrix display. This is ensured by providing a buffer and latch in both the row and column drivers. The Control Logic (CL) synchronizes the display refresh, by generating the appropriate address and control signals using a clock.

b) Approach to Realization

The possible realization of the various blocks along with alternatives, if any, are discussed below.

- Character Generator (CG)

The segment or pixel information of the alphanumeric characters is stored in the CG. An UV-EPROM, EEPROM or ROM could be used here depending on the application.

- Sequence Generator (SG)

An N-bit binary counter generates all the 2^N combinations of row-select patterns required for the BAT. However, the frequency of the counter outputs (row waveforms) increases from MSB to LSB by a factor of two for each bit. This large variation in the frequency of the row addressing waveforms will lead to brightness non-uniformity of the pixels (contrast variation) as discussed in section 2.4.3. While the use of Gray-code will be helpful to reduce frequency variation in the row waveforms, the Pseudo

Random Binary Sequence (PRBS) is a better alternative for the SG. The PRBS and its delayed versions have identical wave shape and hence identical frequency components. But, these sequences have only (2^N-1) states and they do not include the state with all zeros. A sequence generator with all the 2^N states can be obtained by inserting the state with N zeros in the PRBS generator [79]. Such a sequence generator for two values of N, viz., N = 3 and 5 are shown in Fig.4.2 as examples.

- Column Signal Generator (CSG)

The row-select and the data patterns are compared bit-by-bit using Exclusive-OR gates. The column voltage is decided using a majority decision as discussed in section 3.1.2. The majority decision can be implemented using gates, multiplexers or adders. Programmable Logic Array (PLA) and UV-EPROM are the other possible alternatives for the CSG. Here, both the bit-by-bit comparison and the majority decision can be absorbed into a single block.

- Alternatives for CG and CSG

The CG and CSG can be combined into a single block and can be realized using a single ROM, UV-EPROM or EEPROM. The column signal can be directly stored for all the combinations of row-select patterns, column data and the characters.

- Drivers

Driver ICs commonly used for directly driven displays are suitable for BAT. The schematic of a typical driver IC is shown in Fig.4.3. The

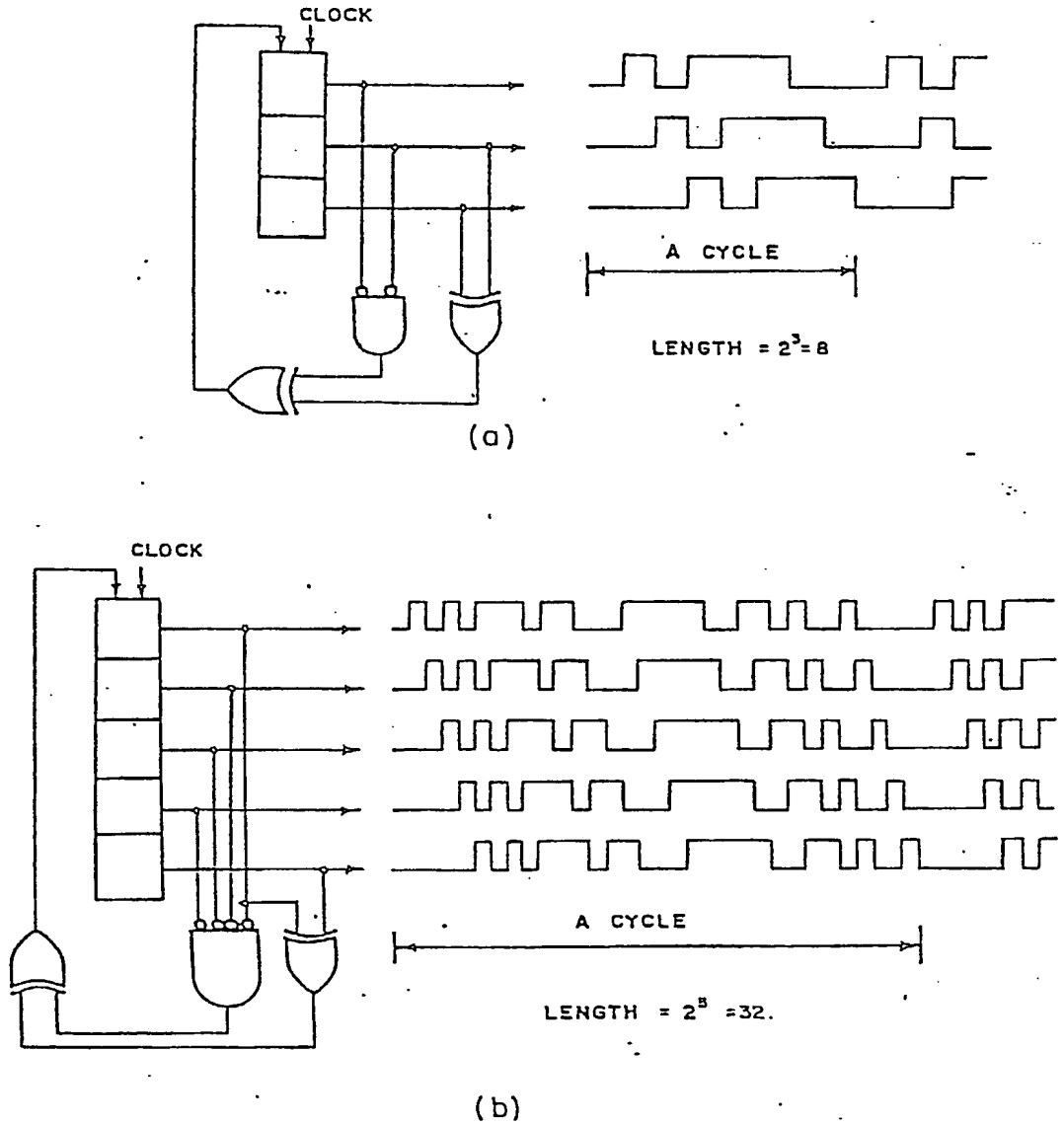


Fig. 4.2. Sequence generators for N = 3 and 5.

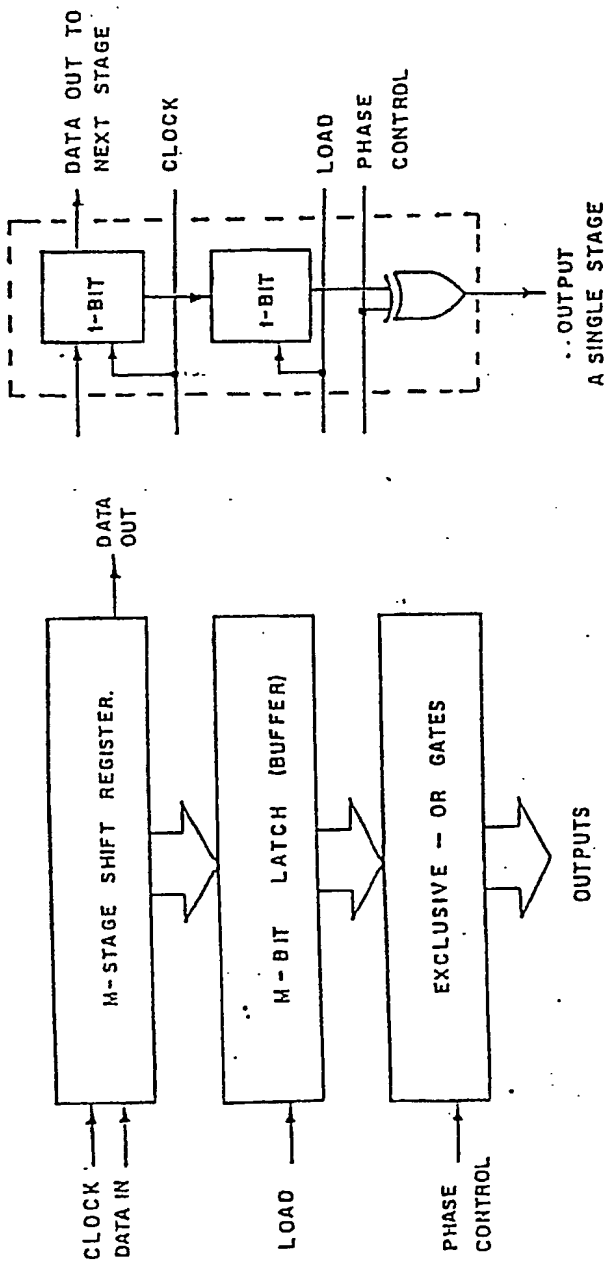


Fig. 4.3. Schematic of a typical driver IC used in directly driven displays.

Exclusive-OR gates are provided to enable phase-reversal, in order to ensure a dc-free operation. But, as the BAT has a natural dc-free operation (as discussed in section 3.1) the phase control input of the EX-OR gates can be permanently tied to logic 0 or 1. Alternatively, the drivers can be implemented using shift registers and latches. The length of the shift register and the number of latches required in the row and column drivers is equal to the number of row and column address lines respectively.

4.1.2. Hybrid Addressing Techniques (HATs)

The HAT (see Appendix 6.b) 1HAT, 1HAT-S3 and 1HAT-S4 discussed in chapter 3 have many common features, since they are based on the same principle. The basic difference between these techniques is the number of voltage levels in the column waveforms as shown in Table 3.19. Hence the block diagram and the approach to realization of the different versions of HAT are discussed here.

a) Block Diagram

The block diagram of the display system using HATs is shown in Fig. 4.4. The information to be displayed is stored in the memory and this can be updated through the interface. The data to be displayed in the selected sub-group of rows (l rows) is loaded into the Re-Circulating Register (RCR) temporarily, for comparing it with the row-select pattern. Hence the size of this register is $l \times M$ bits. The Sequence Generator (SG), generates 2^l, l-bit row-select patterns, for selecting l address lines in the selected sub-group. The Column Signal Generator (CSG) compares the column data pattern in the selected sub-group of rows bit-by-bit with the

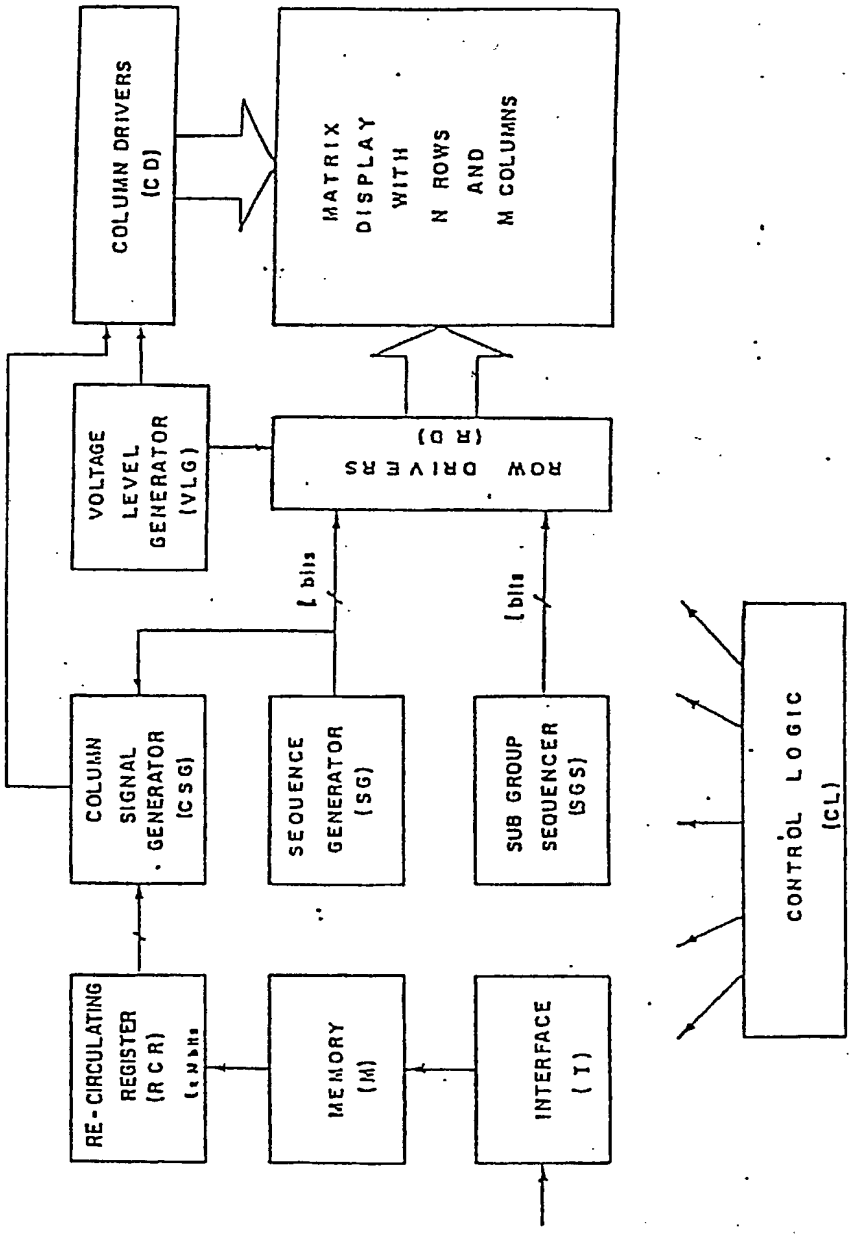


Fig. 4.4. Block diagram of the display system using HATs.

row-select pattern and generates the data for the column drivers. The Sub-Group Sequencer (SGS) determines the l address lines to be selected with voltages corresponding to the l-bit row-select pattern. The data in the RCR corresponds to these selected address lines. The Voltage Level Generator (VLG) is used to generate the various voltage levels in the row and column addressing waveforms. The Row Drivers (RD) are connected to the row address lines of the display and the row voltages are controlled by the row-select pattern obtained from SG and SGS. The Column Drivers (CD) are connected to the column address lines and the column voltages are controlled by the column signal from the CSG. The control logic governs the operation of the various sub-blocks described above and synchronizes the flow of information for refreshing the display.

This block diagram is common for the hybrid addressing techniques, viz., HAT, lHAT, lHAT-S3 and lHAT-S4 discussed in chapter 3. The primary difference between these techniques is the number of voltage levels in the column waveform.This gives rise to different values of relative V_r/V_c for these techniques. The differences in the implementation of the following blocks depend on the particular version of HAT as discussed below:-

- VLG. The number of voltage levels generated for the column drivers depends on the grouping of errors in the addressing technique. The number of voltage levels is 2, $(l+1)$, 3 and 4 for the HAT, lHAT, lHAT-S3 and lHAT-S4 respectively. The relative amplitudes of the column voltages with respect to that of V_r, also depends on the technique as discussed in chapter 3.

- CSG. The number of bits transmitted as signal to the column drivers depends on the addressing technique. The number of bits is 1 for HAT and 2 for 1HAT-S3 and 1HAT-S4. This value depends on l in the case of 1HAT and is $\log_2 (l+1)$, rounded off to the next higher integer when fractions are encountered.

- CD. Analog multiplexers are used in the column drivers to switch the column voltages depending on the signal from CSG. The type of multiplexer required for the addressing techniques are 2 : 1, $(l+1)$: 1, 3 : 1 and 4 : 1 for the HAT, 1HAT, 1HAT-S3 and 1HAT-S4 respectively.

The rest of the blocks, viz., Memory, Interface, RCR, SG, RD and the control logic are common to all the addressing techniques discussed above.

b) Approach to Realization

The possible realization of the various circuit blocks along with alternatives, if any, are discussed below.

- Re-Circulating Register (RCR).

The hybrid addressing techniques require a bit-by-bit comparison of the data to be displayed with the row-select pattern. The RCR facilitates this by storing the data temporarily for repeated comparison with the different row-select patterns. The RCR requires l (= the number of address lines in the selected sub-group) shift registers, each of length M (= the number of columns in the display). Alternatively FIFO (First-In-First-Out) memories can be used along with a feed back for re-circulating the

data. The RCR is provided only for the ease of accessing the same data repeatedly and is optional. An l-bit buffer is adequate, if repeated memory access can be accommodated to fetch the data from the memory.

- Sequence Generator (SG)

The SG generates all the 2^l, l-bit row-select patterns required for selecting a sub-group. The SG can be an l-bit binary counter, Gray code generator or PRBS generator with 2^l states as discussed earlier for BAT. Here again, a Gray code generator or PRBS generator is preferred to achieve the brightness uniformity of the pixels.

- Column Signal Generator (CSG)

The l-bit data from the RCR and the l-bit row-select pattern from the SG are compared bit-by-bit to determine the number of errors. The column voltage depends directly on the number of errors in lHAT. This value is transmitted to the column drivers for a proper choice of the column voltage. The number of column voltages is restricted to 2, 3 and 4 in HAT, lHAT-S3 and lHAT-S4 respectively by grouping of errors in CSG and an appropriate signal is transmitted to the column drivers.

- Voltage Level Generator (VLG)

The various voltage levels required for the chosen addressing technique are generated by potential division using a resistor network as shown in Fig.4.5 for lHAT-S4. The ratio between the amplitudes of the row and column voltages as demanded by the addressing technique is ensured by a proper choice of the value of the resistors. The potentiometer allows for changing the absolute value of the row and column voltages without

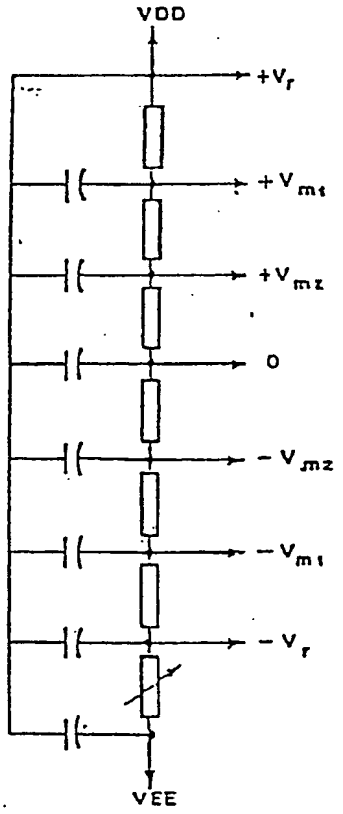


Fig. 4.5. A typical ULG. (IHAT - S4)

altering their ratios. Optional buffer amplifiers can be used for the row and column voltages to reduce the source impedance and is especially useful in large-area displays.

- Column Drivers (CD)

Analog multiplexers are used in the column drivers to switch the different voltages depending on the signal from the CSG. The schematic of a typical CD for HATs is shown in Fig. 4.6. The column signal from the CSG is serially shifted into the shift register. The number of bits (n_c) for each column driver depends on the addressing technique. The value of n_c is 1 for HAT, $\log_2 (\ell+1)$ rounded off to the next higher integer for 1HAT and 2 for 1HAT-S3 and 1HAT-S4. The length of these registers is equal to the number of columns in the display, i.e., M. The row-select pattern applied to the selected subgroup and the column voltages are synchronized using a buffer register. The size of the buffer register is the same as that of the shift register. Analog multiplexer of the types 2:1, $(\ell+1)$: 1, 3:1 and 4:1 are required for HAT, 1HAT, 1HAT-S3 and 1HAT-S4 respectively to drive each column in the display. The column voltages are derived from the ULG.

- Row Drivers

The HATs require one of the three voltages, viz., $-V_r$, 0 and $+V_r$ (or 0, V_r and $2V_r$ for unipolar addressing waveforms.) These voltages are switched using a 3:1 analog multiplexer. The rows in the unselected subgroups get a voltage 0 and this is controlled by a single bit from the SGS. The voltages $\pm V_r$ to be applied to the rows in the selected subgroup are

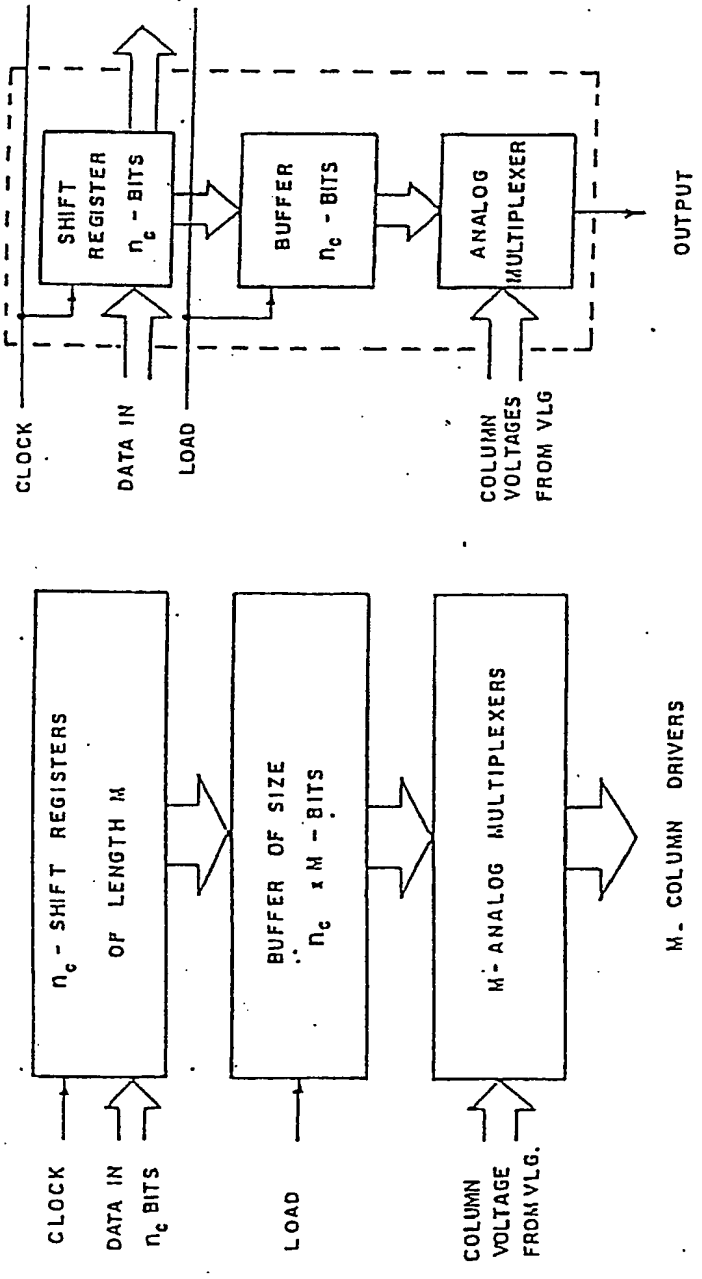


Fig. 4.6. Schematic of a typical column driver for HATs.

controlled by an additional bit for each row from the Sequence Generator. Alternatively the row-select pattern from the SG can be level shifted to $\pm V_r$. Only a 2:1 multiplexer controlled by SGS is required here as compared to a 3:1 multiplexer in the previous case. The total number of multiplexers required is equal to the number of rows in the display, i.e., N. The three voltage levels required here are derived from the VLG.

- Sub-Group Sequencer (SGS)

The SGS determines the sequence in which the subgroups are selected. This in its simplest form is a ring counter of length (N/l). The SGS can be hardwired for a successive or random selection of the subgroups. However, the control logic should be designed to place the data corresponding to the selected subgroup in the column drivers. A digital de-multiplexer can be used as an alternative to the ring counter.

- Control Logic (CL)

The control logic governs the flow of information and synchronizes the various blocks in the display system. They can be implemented using gates, flip-flops and counters.

4.1.3. RPATs

As already discussed in section 3.6, the selection ratio of RPATs is independent of the matrix size. This enhances the usefulness of LCDs for displaying multiple waveforms in oscilloscopes, Logic Analyzers and other display applications without sacrificing the high resolution required in such displays.

are shown in Fig.4.15. The SG based on Gray code and the sequential scanning of subgroups were found adequate to give a good pixel brightness uniformity (without any contrast variation) as it is evident from the photographs of Fig.4.15. The photographs of a 32 x 32 matrix display (having the same specification of the display addressed with HAT) addressed with 1APT are shown in Fig.4.16 for a comparison. The brightness non-uniformity of pixels addressed with 1APT depends on the image being displayed and this is illustrated in Fig.4.16. This non-uniformity can easily be identified by observing the grey level of the background pixels. The brightness uniformity of the pixels in the display addressed with HAT is superior as compared to that of 1APT although the contrast is lower as compared to that of 1APT as shown in Fig.4.15 and Fig.4.16. Typical addressing waveforms applied to the row and column of the matrix display as well as the typical waveform across the ON and OFF pixels are shown in Fig.4.17. The rms voltage across the ON and OFF pixels were measured using HP 3467A, Logging multimeter capable of measuring true-rms voltages. Fig.4.18 gives the plot of rms voltage (across ON and OFF pixels) vs. supply voltage. The theoretical curves in this plot are obtained using eqns. (3.46) and (3.37). These curves are provided for a comparison with the experimental results. The value of the selection ratio obtained from the measurements agree with the theoretical value within ±1%.

4.2.3 1HAT

The 1HAT is demonstrated using a 64 x 64 matrix TNLCD.

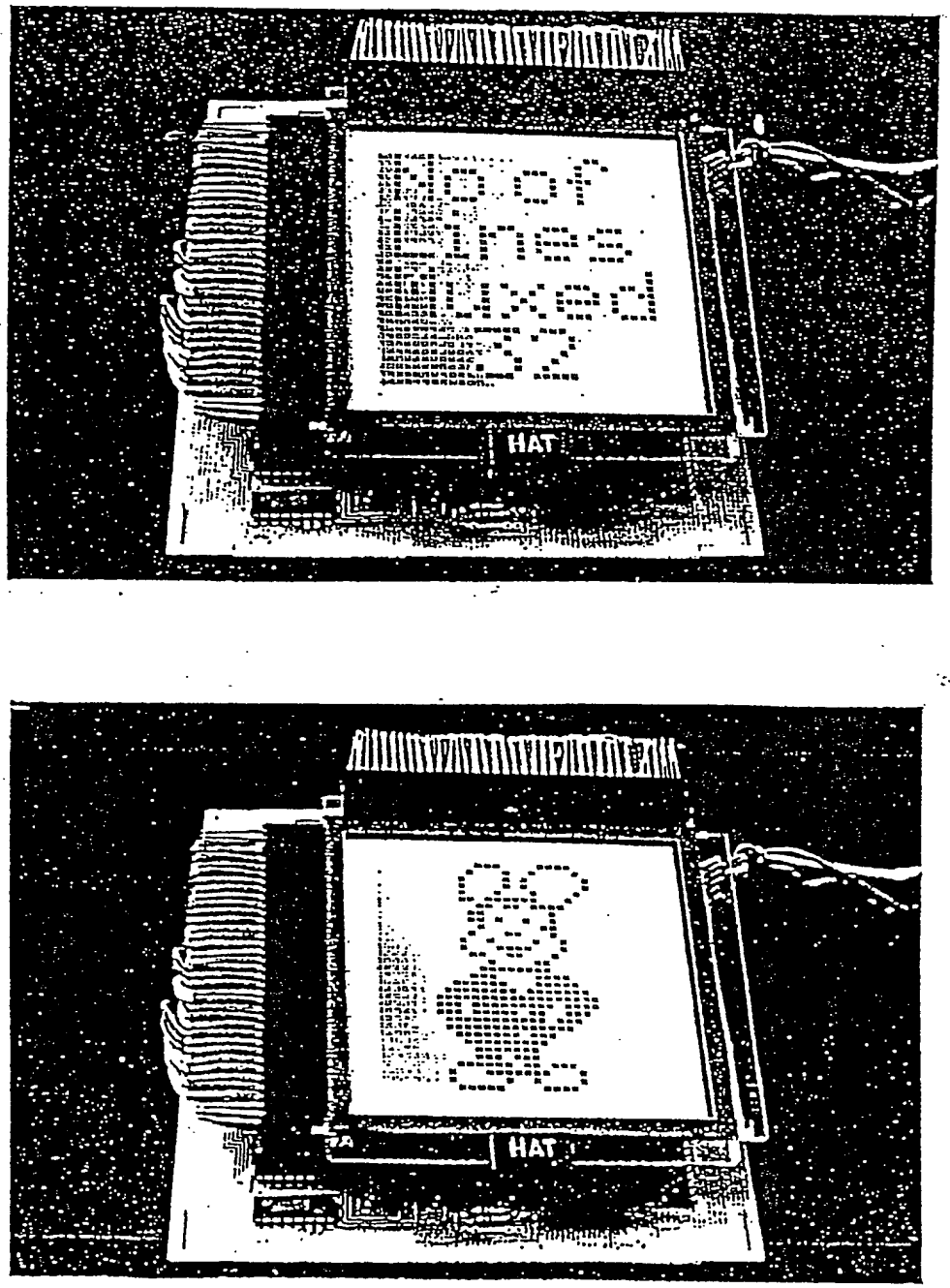


Fig. 4.15. Photographs of a display addressed with HAT (N = 33 and l = 3).

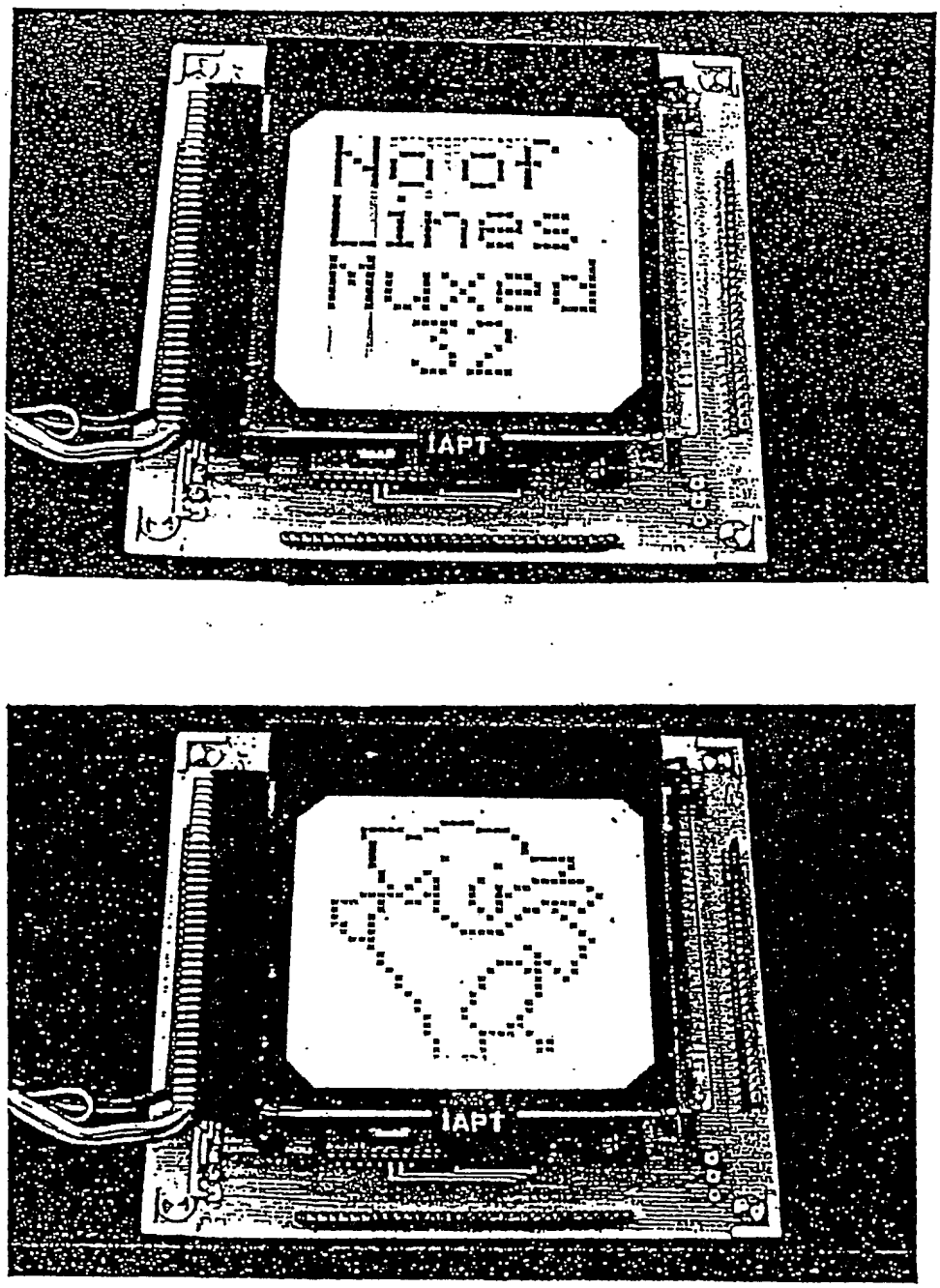
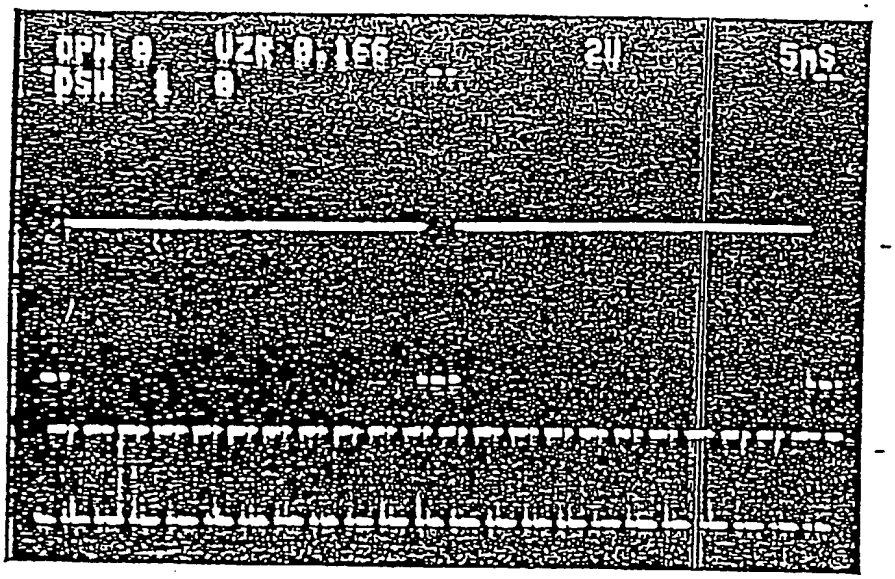
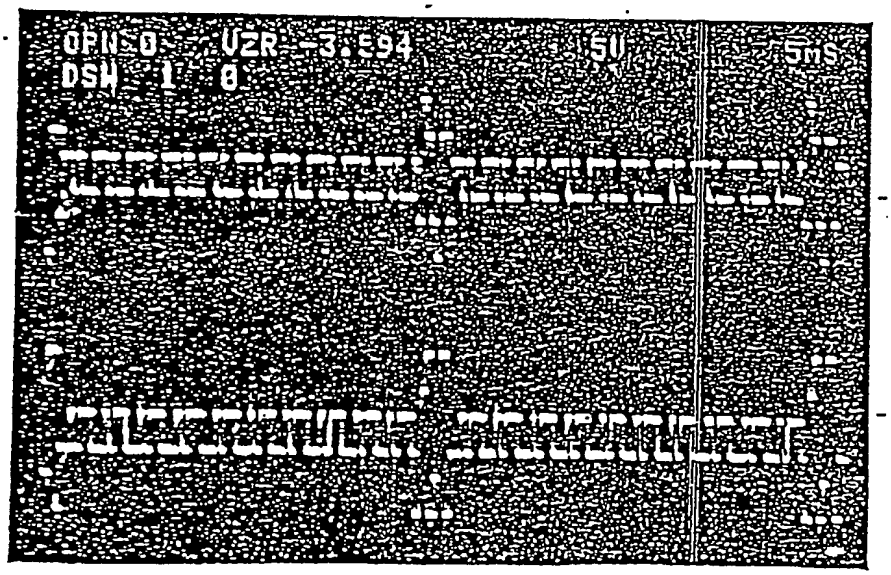


Fig. 4.16. Photographs of a display addressed with IAPT (N = 32).



a) Typical addressing waveforms. WF1 - row and WF2 - column.



b) Typical waveforms across pixels. WF3 - OFF and WF4 - ON.

Fig. 4.17. Waveforms of HAT when $N = 33$ and $l = 3$.

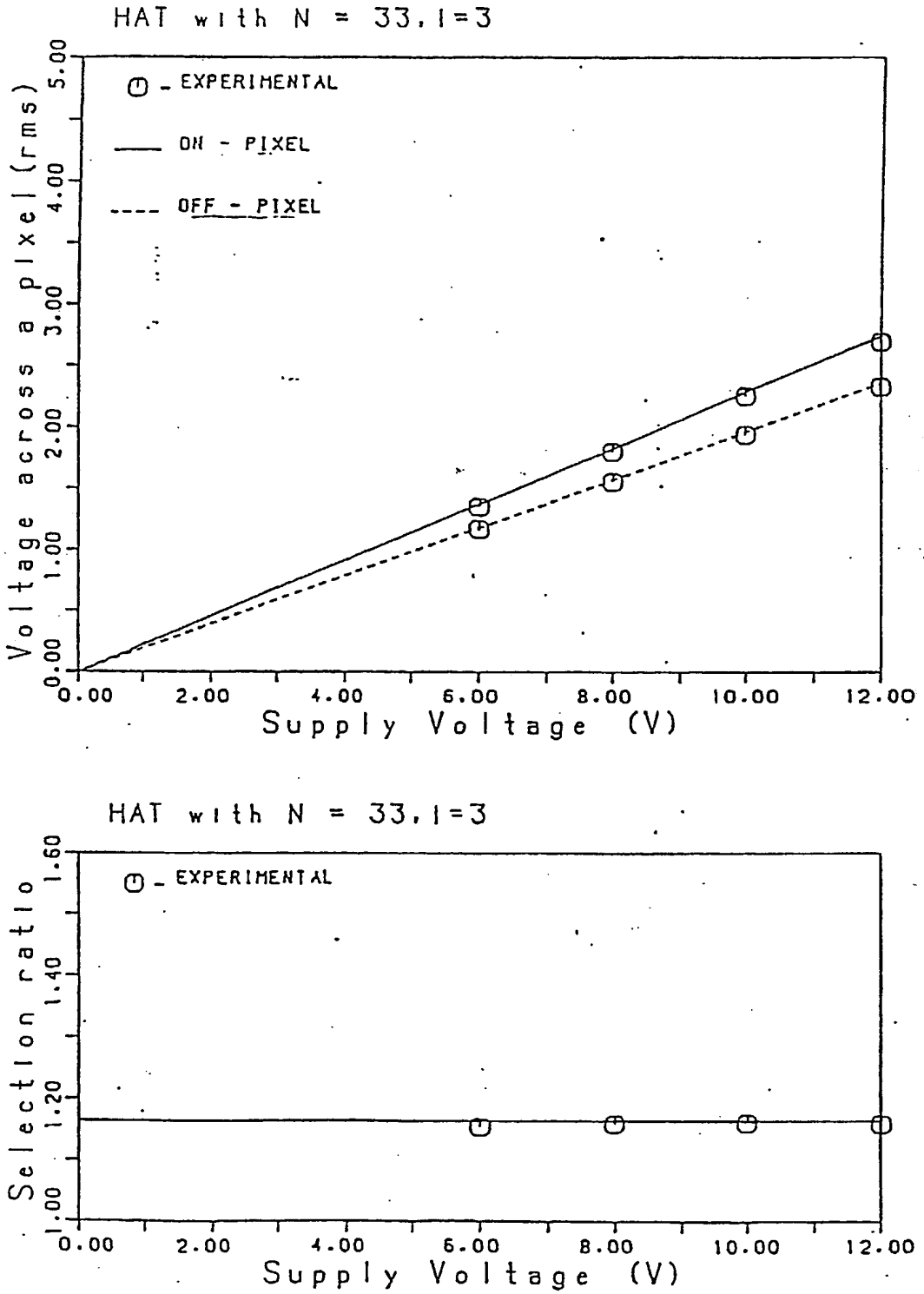


Fig. 4.18. Experimental results of HAT, with N = 33 and l = 3.

a) Display

The specifications of the 64 x 64 matrix TNLCD are given below:-

- Pixel size : 1 x 1 mm
- Active area : 80 x 80 mm
- Connector pitch : 2.54 mm
- Threshold voltage : 1.76 V
- Sharpness parameter : 12.5 %
- Rise time : 66 ms
- Fall time : 50 ms.

The value of l is chosen to be 7 here, since it leads to a good reduction in the supply voltage requirement as shown in Fig.3.6. The value of N, the number of lines multiplexed should be an integral multiple of l as discussed in section 3.3. Hence, N is chosen to be 63, a number close to the number of rows in the matrix display. The selection ratio of IHAT is the same as that of APT or IAPT and hence N_{eq} of IHAT is N, as discussed in section 3.3. The selection ratio is 1.135, for $N=63$. It is evident from the specifications given above, that the value of the sharpness parameter of the NLC mixture is just adequate for this application. The supply voltage requirement of IHAT when $N=63$ as calculated using eqn. (3.99) is 4.538 V_{th}. This value is only 67.13% of the supply voltage requirement of IAPT.

b) Hardware

A detailed block diagram of the display system using IHAT is given in Fig.4.19. The information to be displayed is stored in HN 462532, a

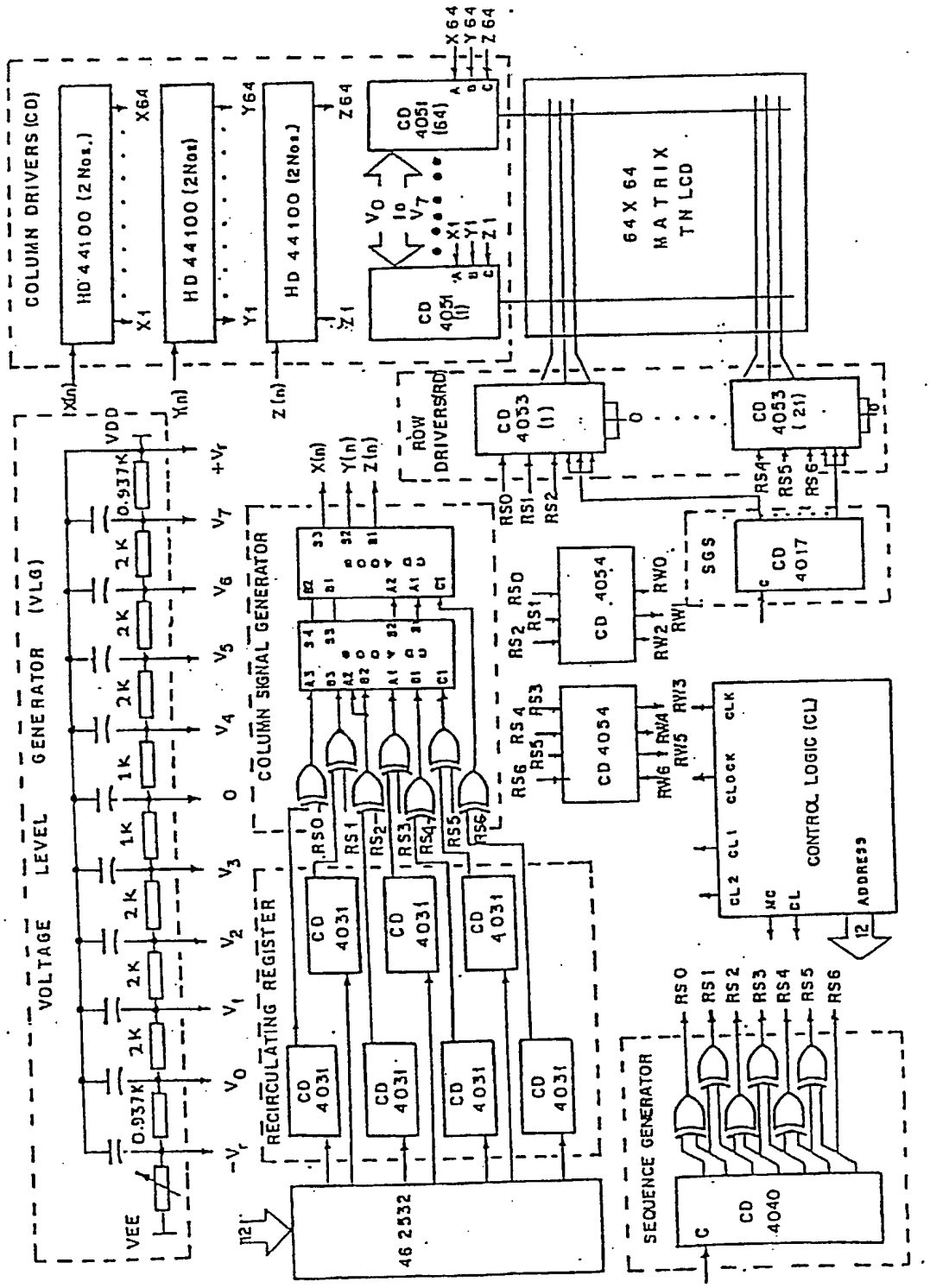


Fig. 4.19. Schematic diagram of a display system using IHAT.

4Kx8-bit UV-EPROM. An EPROM is used here, since the display system is designed only to demonstrate the IHAT. A RAM and suitable interface must be provided in case the display is to be used as a peripheral device. A 7-bit data in a byte of this memory corresponds to the pixel information of a column in a subgroup. This data format eliminates the need for a parallel to serial conversion, which is required if the pixel information is stored row-wise. The first 6-bits of the address input to the memory corresponds to the 64-columns in the matrix display. The next 4-bits correspond to the nine subgroups of rows in the matrix display. The remaining 2-bits are used to select one of the four frames stored in this memory.

The 7-bit parallel data from the memory is loaded into the Re-circulating Register (RCR). This is implemented using seven CD 4031, 64-stage Static Shift Registers. The data in this RCR corresponds to the subgroups of rows to be selected next. The mode-control and the clock for the CD 4031s are generated in the control logic.

The Sequence Generator is implemented using CD 4040, 12-stage Ripple-Carry Binary Counter/Divider and CD 4070, Quad Exclusive-OR Gate as shown in Fig.4.19. The output sequence corresponds to a 7-bit Gray code.

The Column Signal Generator (CSG) is implemented using CD 4070 and CD 4008, 4-Bit Full Adder. The 7-bit output from the RCR is compared bit-by-bit with the row-select pattern (RS0-RS6) using the Exclusive-OR gates. The number of errors (logic 1 at the output of the Exclusive-OR gate) is counted using two CD 4008 as shown in Fig.4.19. The unused input

of the adders are connected to logic 0 and it is important to note that all the inputs to these adders have equal weightage. The 3-bit output, viz., X(n), Y(n) and Z(n) of the adder gives the number of errors (which ranges from 0-7 depending on the row-select pattern and the data to be displayed in a column of the selected sub-group).

The Column Driver consists of sixty-four CD 4051, Triple 2-Channel Analog Multiplexer/Demultiplexer and six HD 44100, LCD Driver with 40-channel outputs. It is important to note that the HD 44100s are used here only to serially shift in the data from the CSG and to latch them in parallel, using the shift register and the latch available in the HD 44100s. They are not used as LCD drivers since HD 44100 can switch only two voltage levels corresponding to the 1-bit data in the latch while the IHAT requires 8-voltage levels to be switched in this application as discussed earlier. The CD 4051 is used to switch one of the eight voltage levels (V_0-V_7) from the VLG.

The row-select pattern is level-shifted using CD 4054 to form the Row waveforms (RW6-RW0). These waveforms are applied to the selected subgroup of rows and their amplitude is either $-V_r$ or $+V_r$ depending on the row-select pattern. The row waveforms are synchronized with the column waveforms by latching the row-select pattern corresponding to the data in the column drivers into the CD-4054 simultaneously as the column data.

Twenty-one CD 4053, Triple 2-channel Multiplexer/Demultiplexer are used as Row Drivers (RD). The CD 4053 either connects one of the row waveforms (RW0-RW6) or the voltage level '0' from the VLG depend-

ing on the control from the Sub-Group Sequencer (SGS). The rows in the selected subgroup are connected to the row waveforms, while the rows in the unselected subgroups are connected to the voltage level 0 as discussed in section 3.3.

The Sub-Group Sequencer (SGS) is implemented using CD 4017, Decade Counter/Divider with 10 Decoded Decimal Outputs. The SGS selects 1 of the 9- subgroup of rows. The SGS is synchronized with the address input of the memory, so that the data in the column drivers corresponds to the selected subgroup.

$N = 63$ $l = 7$

The ratio V_r/V_0 for $N = 63$ is calculated from eqn. (3.84). The relative magnitudes of the column voltage are as per eqn. (3.85) and are shown in Table 3.9. The VLG implemented using trimmed resistors, with their values accurate to ± 1 ohm is shown in Fig.4.19.

Some important signals generated in the Control Logic (CL) for a proper function of the various blocks in the display system are given below:-

- 12-bit address to the HN 462532 for reading the pixel information from the memory.
- CL, the clock to CD 4031s.
- MC, the mode control to the CD 4031s to load the data from HN 462532 or to recirculate the data in the CD 4031s.
- CL2, to HD 44100s to serially shift in the data from the CSG.
- CL1 to load the data into the latch of HD 44100.
- Clock to the CD4040.
- CLK, the clock to CD 4017 .

The CL is hard-wired for the following row-select sequence:-

- Each sub-group is selected with four row-select patterns before the next sub-group is selected.

7 × 9 = 63

- The subgroups are selected sequentially one after the other.

  The CL has flexibility (switch selectable) to change the four row-select pattern either when a new subgroup is selected or at the end of selecting all the nine-subgroups. The subgroups are selected each time for a duration of approximately .1 ms. Although the time required to complete a cycle is approximately 120 ms, no flicker is observed since the subgroups are selected after every 3.6 ms.

3.7 × 9 × 3

c) Results

The photograph of the 64x64 matrix TNLCD, addressed using 1HAT are shown in Fig.4.20. The upper photograph in the figure illustrates the contrast variation in TNLCDs with the viewing angle as well as the intensity of light falling on it. The lower photograph in the same figure illustrates the brightness uniformity of the pixels in the display addressed with 1HAT. Both the scanning sequences discussed above have resulted in a good pixel brightness uniformity. Typical addressing waveforms applied to the row and column of the matrix LCD as well as the waveforms across the ON and OFF pixels are shown in Fig.4.21. The rms voltage across the ON and OFF pixels were measured using HP3467A, a Logging multimeter capable of measuring true-rms voltage. Fig.4.22 gives the plot of rms voltage across the ON and OFF pixels vs. supply voltage. The theoretical curves of this plot are obtained by using eqns. (3.99) and (3.91). These curves are shown

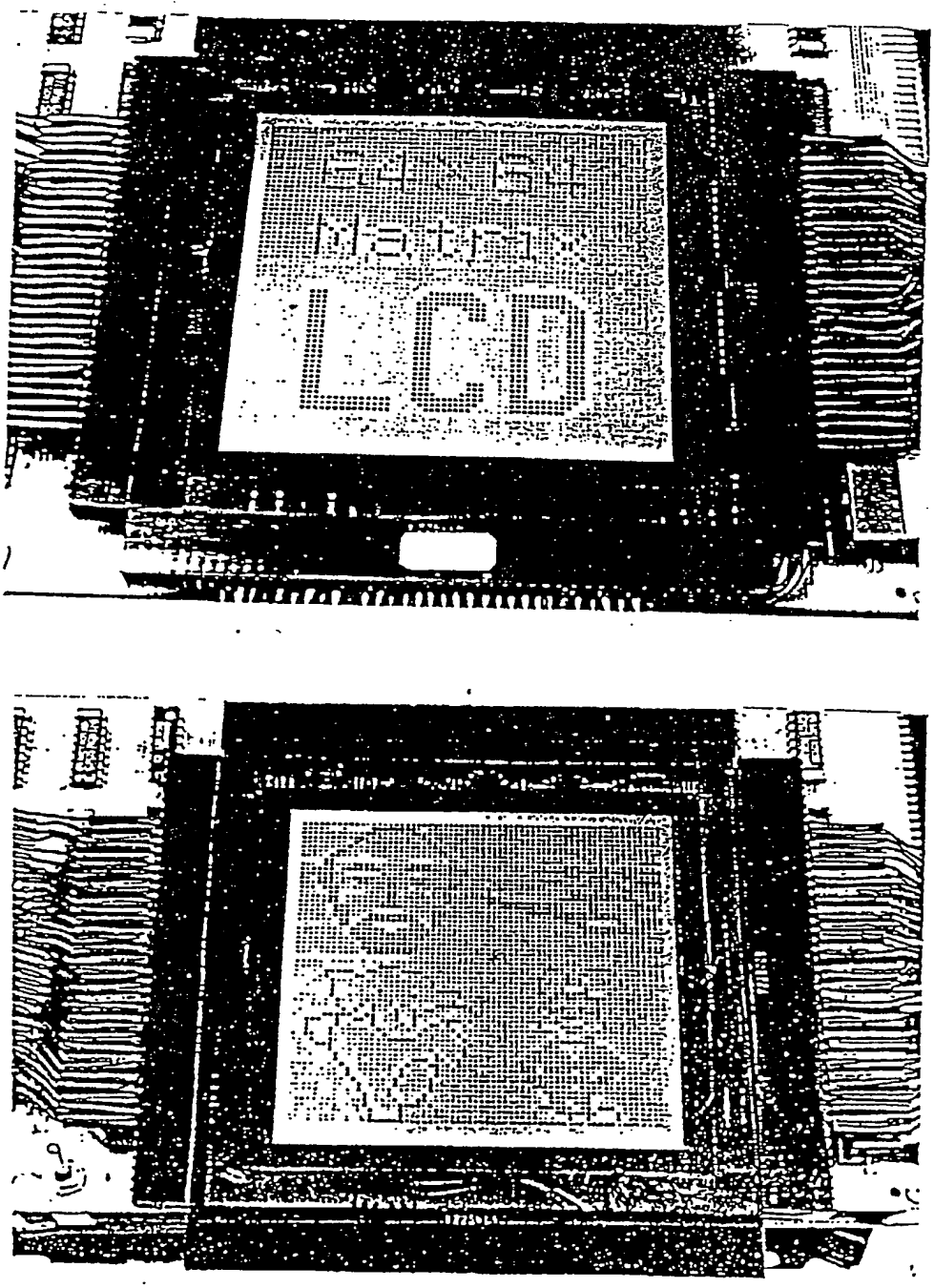
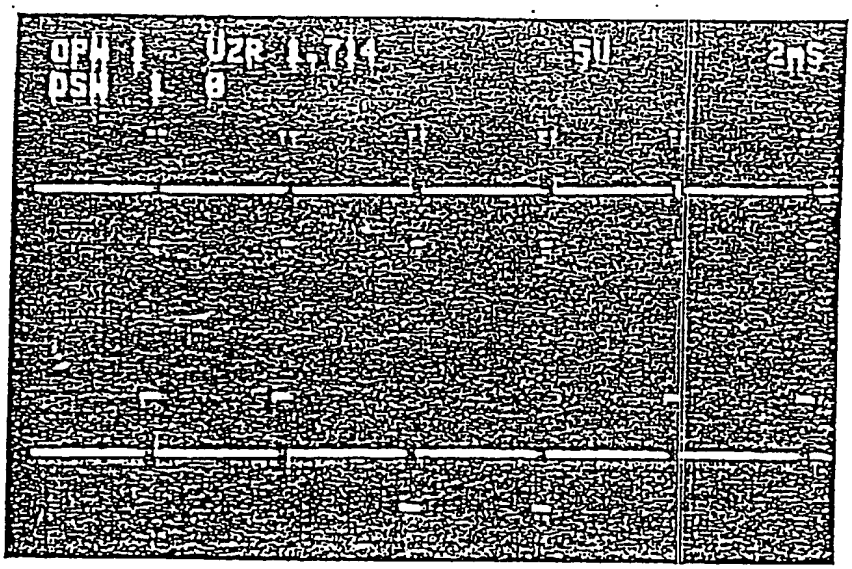
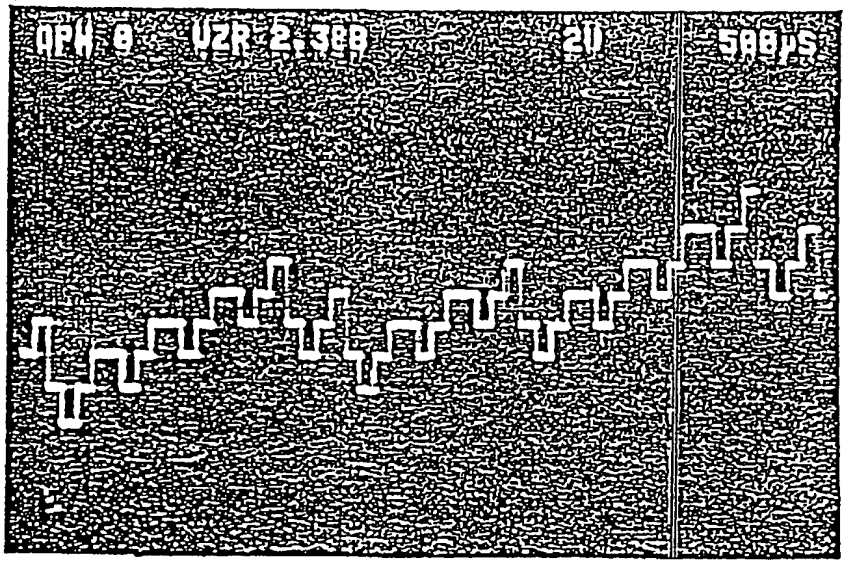


Fig. 4.20. Photographs of a display addressed with IHAT (N = 63 and t = 7).

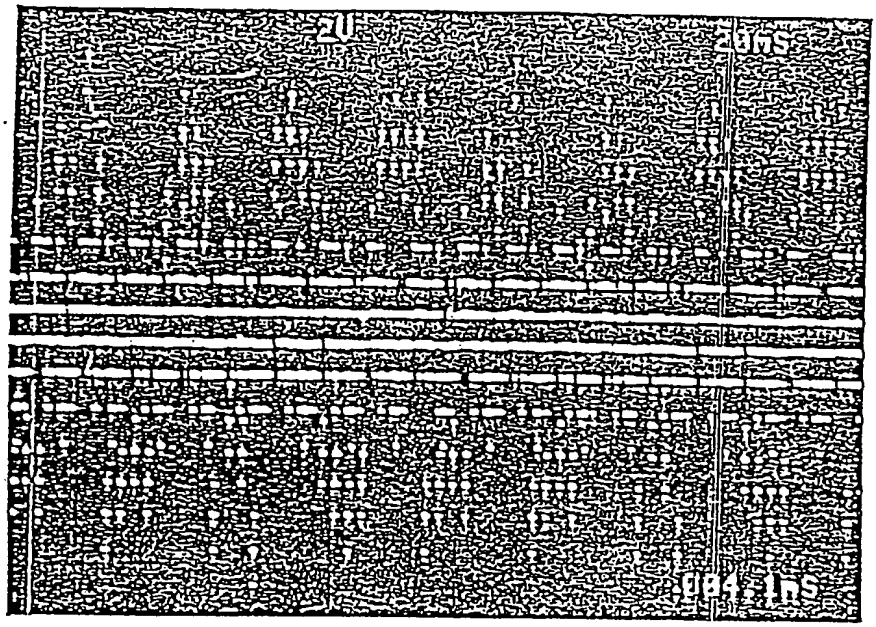


a) Typical row waveforms of IHAT .

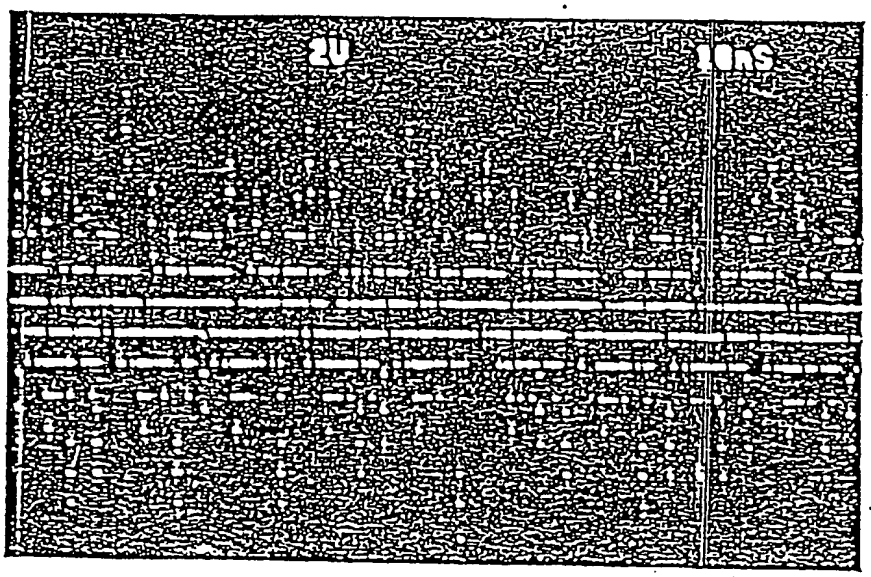


b) Typical column waveform of IHAT .

Fig. 4.21. Waveforms of IHAT when $N = 63$ and $l = 7$.

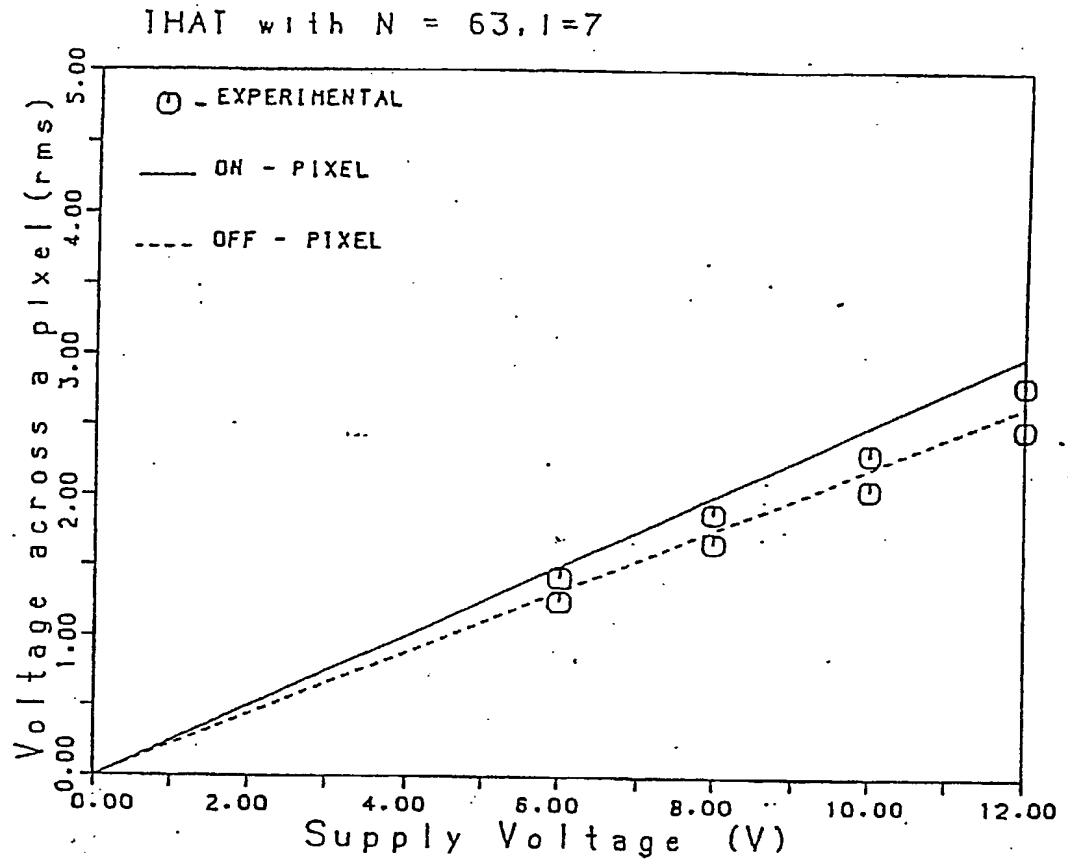


c) Typical waveform across an ON pixel in 1HAT .



d) Typical waveform across an OFF pixel in 1HAT .

Fig. 4.21. Waveforms of 1HAT when $N = 63$ and $l = 7$.



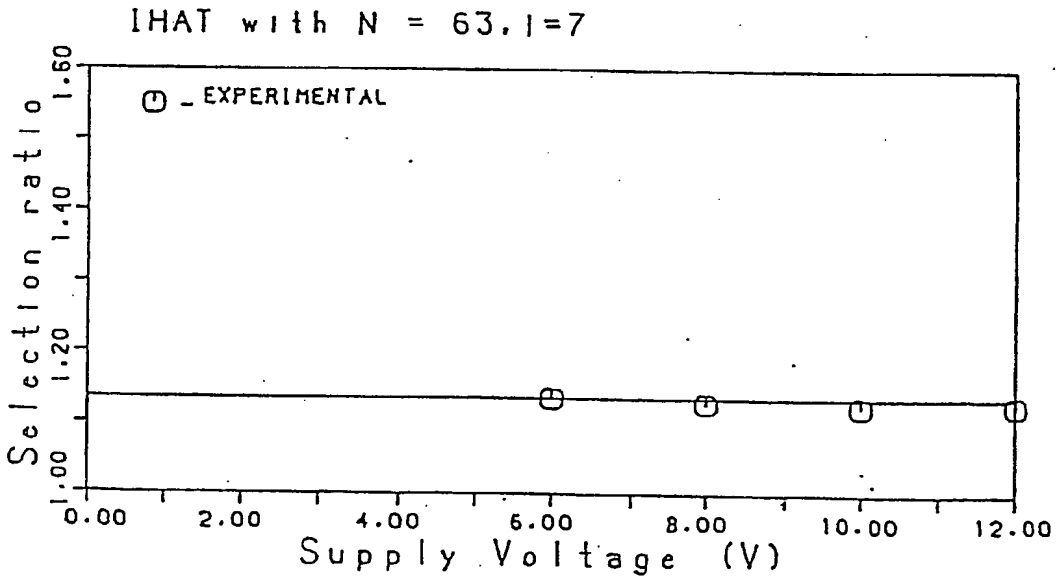


Fig. 4.22. Experimental results of IHAT, with N = 63 and l = 7 .

for comparison with the experimental results. The measured values of the rms voltage across the pixels are lower than the theoretical values. This may be attributed to the limited bandwidth of the measuring instrument. The value of the selection ratio obtained from the measurements agree with the theoretical value within ±1%, although the rms voltage across the ON and OFF pixels are lower than the theoretical values as shown in Fig. 4.22.

4.2.4. IHAT-S4

The IHAT-S4 is demonstrated using a 64 x 64 matrix TNLCD.

a) Display

The specifications of the 64 x 64 matrix TNLCD are the same as that of the display used for the demonstration of IHAT. The value of l is chosen to be 7 so that the results of IHAT and IHAT-S4 can be compared. The value of N is again 63. The best possible value for N_{eq}, when $l=7$ is (232N/215) as shown in Table 3.16. The selection ratio for $N=63$ is 1.130, which is 99.5% of the maximum value possible (using IAPT or IHAT). However the supply voltage requirement of IHAT-S4 is 5.13 V_{th}, which is only 75.9% of that of IAPT (Table 3.18).

b) Hardware

The hardware realization of IHAT-S4 is the same as that of IHAT except for the following blocks:-

- Column Signal Generator (CSG)